YAMAHA LSI S-3527

NO.85-04

S-3527

MSX System (MSX Port Controller and Software Controlled Sound Generator)

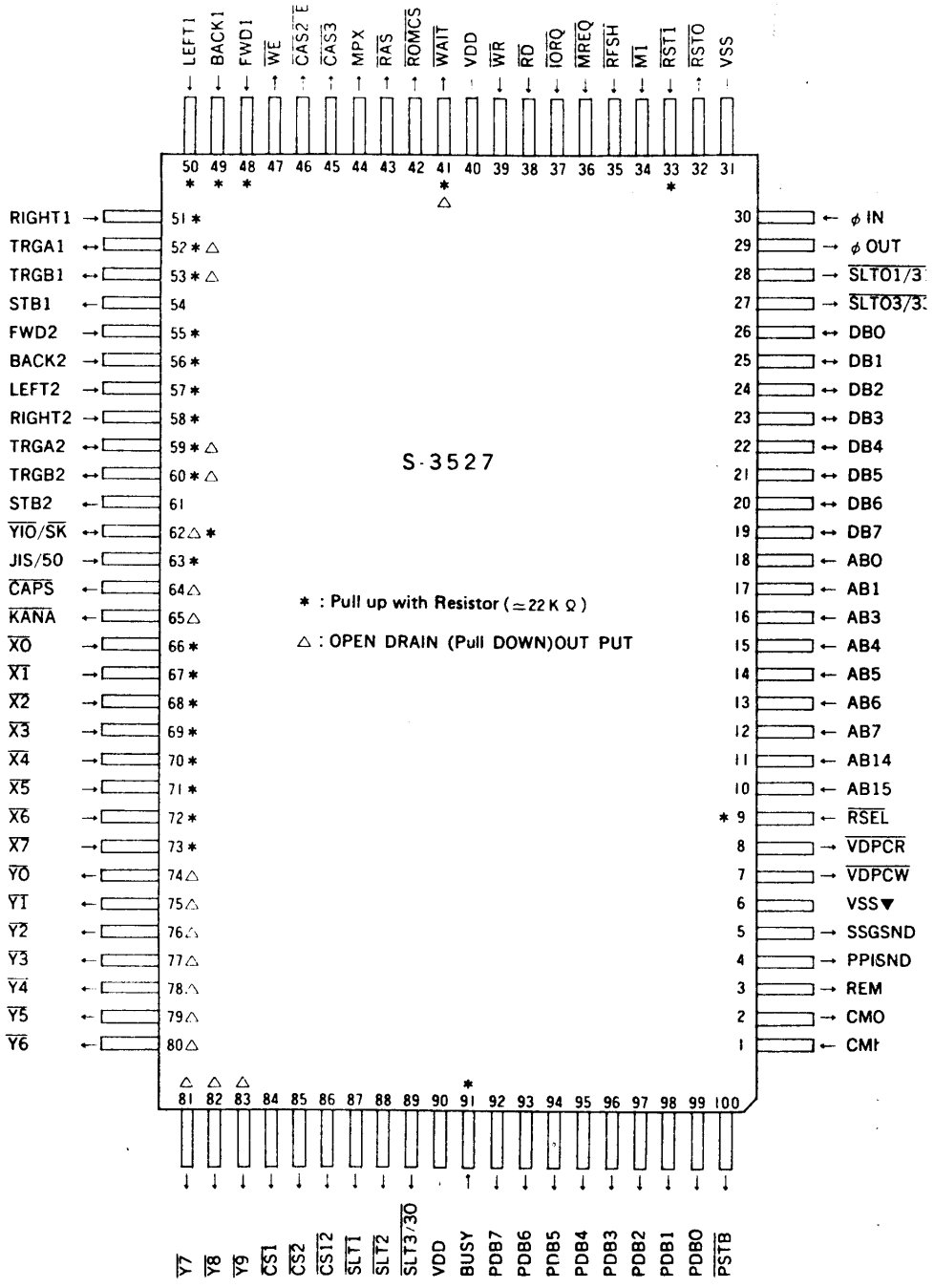
■ OUTLINE

YAMAHA S-3527 is an LSI developed for MSX computers. According to MSX specifications, it controls access to basic and expanded memories, VDP, keyboard, and peripheral devices like a printer. It incorporates SSG which is capable of generating music sound signals.

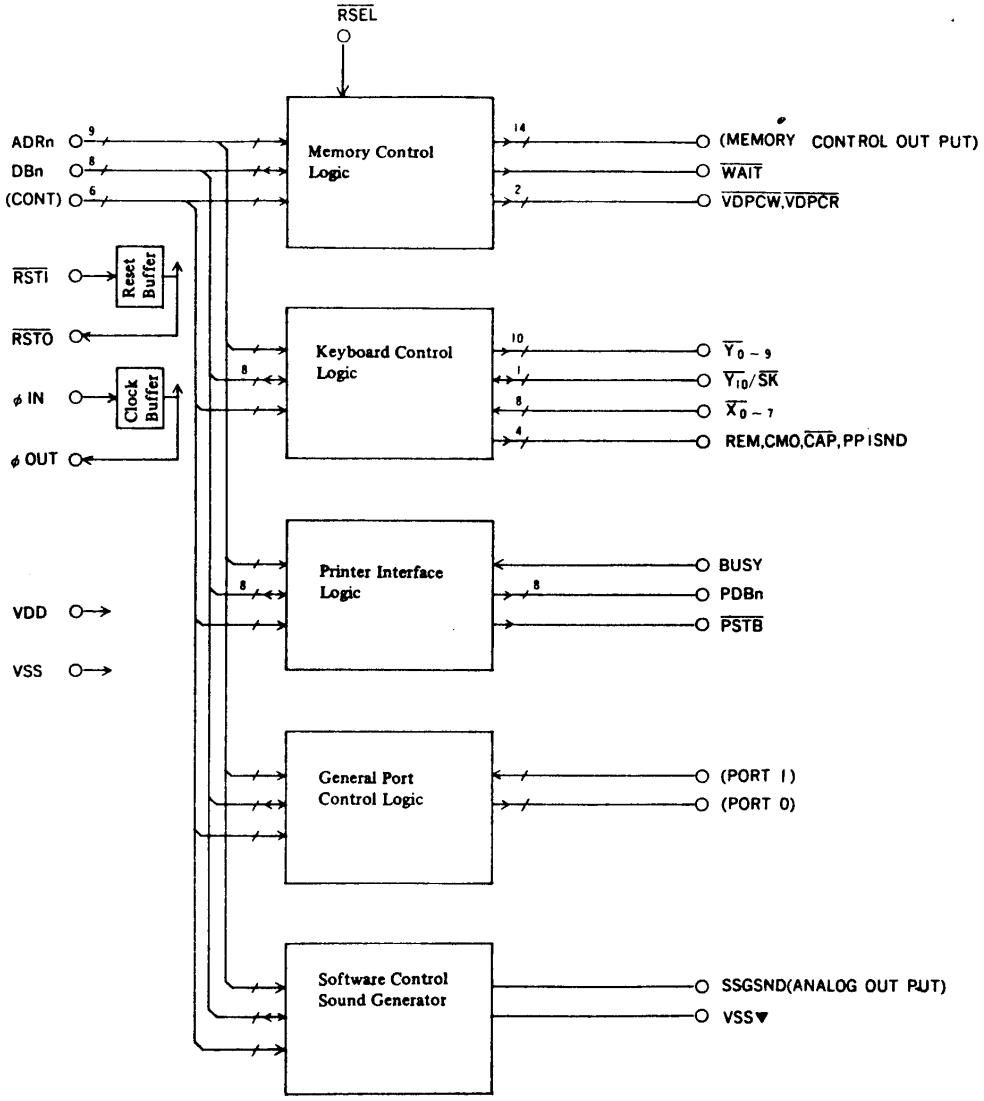
■ FEATURES

- Access to ROM (MSX BASIC ROM: 32 Kbyte)
- Access to RAM (D-RAM: 16K–16 Kbyte or 64 Kbyte when expanded)
- Control of basic slots
- Selecting and controlling expansion slot
- Insertion of 1WAIT during M1 cycle
- Access to keyboard (including numeric key pad)
- Incorporates two joysticks (or general ports)
- Incorporates SSG (equivalent of YAMAHA YM-2149)
  - Sound range: 8 octaves
  - Sound types: 3-channel square waves and 1-channel noise
  - Envelope control: 5 bits
  - D/A converter : 5 bits
- CMOS device with Si gate
- Driven by +5V alone
- 100-pin plastic flat package

■ PIN ASSIGNMENT



■ BLOCK DIAGRAM



(CONT): M1, RFSH, MREQ, IORQ, RD, WR

(MEMORY CONTROL OUT PUT): ROMCS, RAS, MPX, CAS3, CAS2 E, WE, CS1, CS2, CS12, SLT1, SLT2, SLT3 30, SLT01 31, SLT03:33

(PORT 1): FWD1, FWD2, BACK1, BACK2, LEFT1, LEFT2, RIGHT1, RIGHT2, (TRGA1, TRGA2, TRGB1, TRGB2) ( ) : Wired Logic i/o

(PORT 0): (TRGA1, TRGA2, TRGB1, TRGB2) STB1, STB2

■ PIN FUNCTIONS

Pin Name	I/O	Function
(AB15, AB14 / AB7 ~ AB3 / AB1, AB0)	i	Z80A CPU address bus in (9 bits)
DB7 ~ DB0	i/o	Z80A CPU data bus in/out (8 bits)
$\overline{M1}$	i	Z80A CPU $\overline{M1}$ in
$\overline{RFSH}$	i	Z80A CPU $\overline{RFSH}$ in
$\overline{MREQ}$	i	Z80A CPU $\overline{MREQ}$ in
$\overline{IORQ}$	i	Z80A CPU $\overline{IORQ}$ in
$\overline{RD}$	i	Z80A CPU $\overline{RD}$ in
$\overline{WR}$	i	Z80A CPU $\overline{WR}$ in
$\overline{WAIT}$	o	1WAIT request signal out during M1 cycle (possible to wired-OR with external WAIT signal)
$\overline{ROMCS}$	o	MSX BASIC ROM select signal out
MPX	o	D-RAM address multiplexing signal out
$\overline{RAS}$	o	D-RAM $\overline{RAS}$ signal out (RAS-only refresh possible by Z80)
$\overline{CAS2/E}$,$\overline{CAS3}$	o	D-RAM $\overline{CAS}$ signal out { CAS3 : SLOT ≠ 0 C000 ~ FFFF or SLOT ≠ 00 C000 ~ FFFF / CAS2 E : SLOT ≠ 0 8000 ~ BFFF or SLOT ≠ 00 8000 ~ BFFF / or SLOT ≠ 02 0000 ~ 7FFF or SLOT ≠ 32 0000 ~ FFFF }
$\overline{WE}$	o	D-RAM $\overline{WE}$ signal out
$\overline{CS1}$,$\overline{CS2}$,$\overline{CS12}$	o	ROM select signal out ($\overline{CS1}$: 4000-7FFF $\overline{CS2}$: 8000-BFFF $\overline{CS12}$: 4000-BFFF)
$\overline{SLT1}$,$\overline{SLT2}$,$\overline{SLT3\ 30}$	o	Slot select signal out ($\overline{SLT1}$: SLOT ≠ 1 $\overline{SLT2}$: SLOT ≠ 2 $\overline{SLT3\ 30}$: SLOT ≠ 3 or SLOT ≠ 30)
$\overline{SLT01\ 31}$	o	Expansion slot # 01 or # 31 select signal out
$\overline{SLT03/33}$	o	Expansion slot # 03 or # 33 select signal out
$\overline{RSEL}$	i	Expansion slot select register control signal in
$\overline{VDPCR}$	o	VDP (video display processor) read timing signal out
$\overline{VDPCW}$	o	VDP write timing signal out
PDB7 ~ PDB0	o	Print data out (8 bits)
$\overline{PSTB}$	o	Printer strobe out

Pin Name	I/O	Function
BUSY	i	Printer status in
$\overline{X7}$ ~ $\overline{X0}$	i	Keyboard return signal in (8 bits) ($\overline{X6}$ and $\overline{X7}$ receive function select signal when reset.)
$\overline{Y9}$ ~ $\overline{Y0}$,($\overline{Y10}$/$\overline{SK}$)	o(o/i)	Keyboard scan signal out (11 bits) ($\overline{Y10}$ / $\overline{SK}$ receive serial key signal by selected function when reset.)
FWD1,FWD2	i	Joystick FWD signal or general port signal in
BACK1,BACK2	i	Joystick BACK signal or general port signal in
LEFT1,LEFT2	i	Joystick LEFT signal or general port signal in
RIGHT1,RIGHT2	i	Joystick RIGHT signal or general port signal in
TRGA1,TRGA2	i/o	Joystick TRGA signal or general port signal out (I/O by wired logic)
TRGB1,TRGB2	i/o	Joystick TRGB signal or general port signal out (I/O by wired logic)
STB1,STB2	o	General port signal out
CMI	i	Cassette tape read signal in
CMO	o	Cassette tape write signal out
REM	o	Cassette tape control signal out
$\overline{CAPS}$	o	CAPS lamp signal out (drives LED directly)
$\overline{KANA}$	o	Kana lamp signal out (drives LED directly)
JIS/50	i	Keyboard arrangement control signal in
$\overline{RSTI}$	i	Reset signal in (input to Schmitt)
$\overline{RSTO}$	o	Reset signal out
PPISND	o	Software-defined sound out
SSGSND	o	SSG-generated analog sound out
ϕ IN	i	Clock in (This is used via a buffer except for Z80A.)
ϕ OUT	o	Clock for Z80A CPU out
VDD		+5V power
VSS		0V GND
VSS▼		0V SSG GND

■ DESCRIPTION OF FUNCTIONS

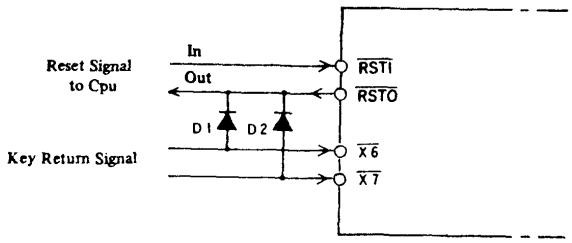
> Selection of Function and Initialization

When the reset signal has come, it is possible to select an expansion slot and assign the numeric key drive signal output terminal ($\overline{Y10}$ / $\overline{SK}$) to receive serial keyboard signal, using $\overline{X6}$ and $\overline{X7}$ out of the keyboard return signal input terminals. As the sample circuit below shows, function is selected by the presence or absence of diodes D_1 and D_2 across the reset signal output terminal ($\overline{RSTO}$) and the keyboard return signal input terminals. Memory maps shown on the next page indicate how expansion is realized.

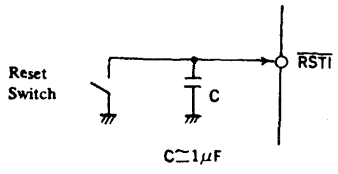
$\overline{X6}$ and $\overline{X7}$ input levels on initialization and functions

$\overline{X6}$	$\overline{X7}$	Function	Diodes
0	X	Slot 0 expansible	D1 installed
1	X	Slot 3 expansible	D1 removed
X	0	Serial key circuit works	D2 installed
X	1	Numeric key driver works	D2 removed

Function select circuit sample

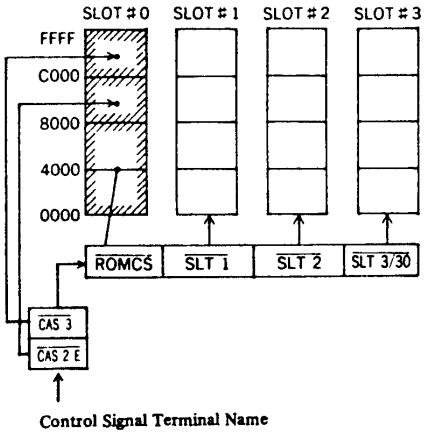


The reset signal applied to the $\overline{RSTI}$ terminal may be either the source voltage or can be generated with a capacitor connected to the $\overline{RSTI}$ terminal as shown below.
To reset the device, the $\overline{RSTI}$ signal should remain at "0" level for more than 20 times of the clock cycle when the source voltage has risen sufficiently and the clock signal is supplied.

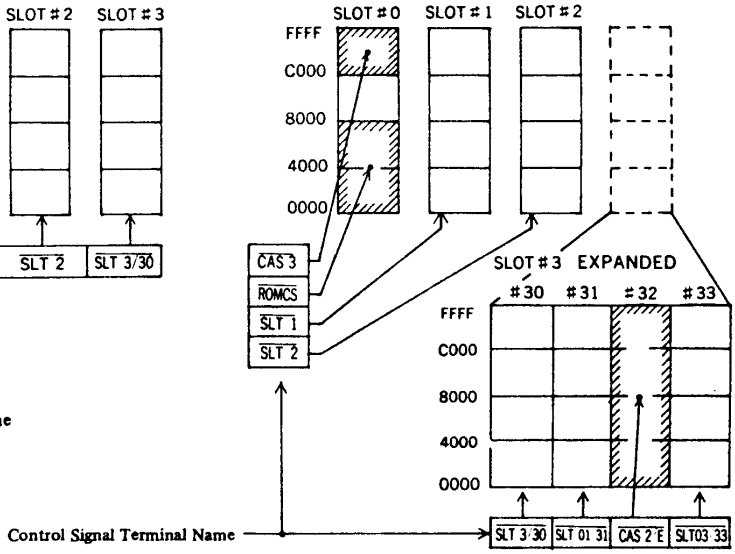


Memory maps and expansion

(Unexpanded)

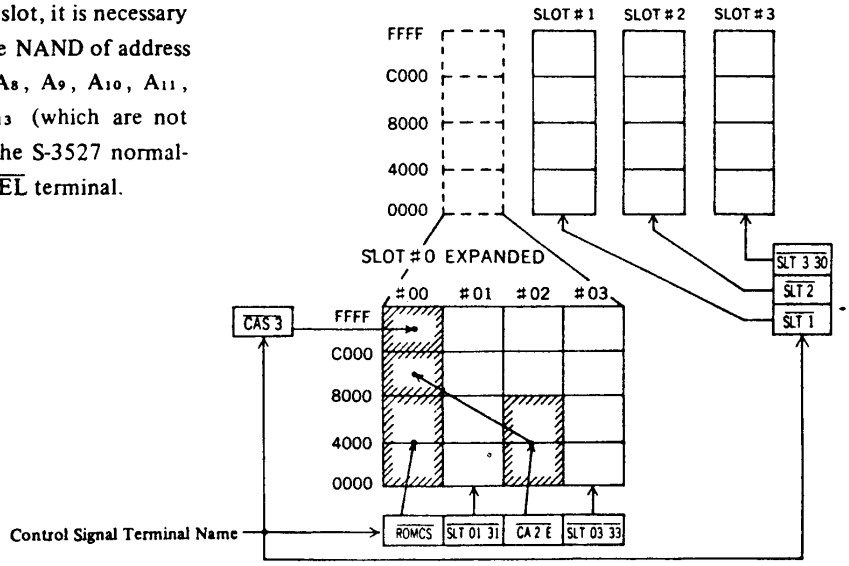


(Slot # 3 is expanded)



(Slot # 0 is expanded)

To expand a slot, it is necessary to supply the NAND of address signals A_2, A_8, A_9, A_{10}, A_{11}, A_{12}, and A_{13} (which are not supplied to the S-3527 normally) to the $\overline{\text{RSEL}}$ terminal.



> Memory Control Signals

Refer to the timing diagrams given in the section of electrical characteristics for logic levels and timing of the system control signals ($\overline{M1}$, $\overline{RFSH}$, $\overline{MERQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$) coming from the CPU, memory control output signals ($\overline{ROMCS}$, $\overline{RAS}$, $\overline{MPX}$, $\overline{CAS3}$, $\overline{CAS2 / E}$, $\overline{WE}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS12}$, $\overline{SLT1}$, $\overline{SLT2}$, $\overline{SLT3 / 30}$, $\overline{SKT01 / 31}$, and $\overline{SLT03 / 33}$), CPU memory signal ($\overline{WAIT}$), and VDP control signals ($\overline{VDPCR}$ and $\overline{VDPCW}$).

> I/O Addresses and Functions

The functions of printer, VDP, SSG, general ports, keyboard, and slot select are fixed with I/O addresses given as shown below according to the MSX specifications.

I/O addresses and functions

Function	I/O ADR	W/R	Description
Printer	90 (HEX)	W	Printer strobe out from $\overline{PSTB}$ (Bit 0)
	90	R	Printer status in to BUSY (Bit 1)
	91	W	Print data out from PDB0 ~ 7 (Bits 0 ~ 7)
VDP	98	W	VDP write timing signal out from $\overline{VDPCW}$
	99	W	
	98	R	VDP read timing signal out from $\overline{VDPCR}$
	99	R	
SSG and general ports	A0	W	Address latch
	A1	W	Data write
	A2	R	Data read
Keyboard and slot select	A8	W	Slot select signal register data write
	A8	R	Slot select signal register data read
	A9	R	Keyboard return signal read
	AA	W	Keyboard drive signal register write
	AA	R	Keyboard drive signal register read
	AB	W	Mode select

> Bit assignments of keyboard and slot select registers

Function	Bit	W/R	Description	
Slot select register	0 1	W/R	Select signal of 0000-3FFF slot	
	2 3		Select signal of 4000-7FFF slot	
	4 5		Select signal of 8000-BFFF slot	
	6 7		Select signal of C000-FFFF slot	
Keyboard return	0 1 2 3 4 5 6 7	R	Keyboard return signal	
Keyboard drive register	0 1 2 3	W/R	Keyboard drive signal (0 ~ 10 decoded from the four bits are output to $\overline{Y0}$ ~ $\overline{Y9}$ and $\overline{Y10}$ / $\overline{SK}$.)	
	4		Cassette tape control REM signal	
	5		Cassette tape write CMO signal	
	6		$\overline{CAP}$ signal for CAPS lamp	
	7		Software-generated sound signal PPISND	
Mode select	0 1 2 3 4 5 6 7	W	0 1 0 0 0 0 0 1	When bit 7 is level "1", slot select and keyboard drive registers will be cleared. This is just like mode 0 of 8255A that ports PA and PC are assigned to output and port PB to input.
	0 1 2 3 4 5 6 7	W	B_0 B_1 B_2 B_3 0 0 0 0	When bit 7 is level "0", each bit of keyboard drive registers can be set or reset. B_1 ~ B_3 indicate bit No. Its content will be set when B_0 is 1 and reset when 0.

> SSG and general ports

SSG is controlled by 14 registers (register contents can be read without affecting sounds). Sounds are generated with three 8-octave square wave generators, a pseudo-random noise generator, a a 5-bit envelope generator for single-shot and repeated attenuation, a sound level controller, a mixer of music sounds and noises, and a 5-bit D/A converter.
The general ports include an output port and an input port connected to registers.

Register array

When high-order DB7 ~ DB4 of 8-bit address signal are 0 (H), low-order DB3 ~ DB0 (4 bits) select 15 registers. The address, once read, is retained, kept unaffected by data read/write, until a new address is given.
The register array is as follows.

Register array

Register	Address (H)	Function \ Bit	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
R_0	00	Channel A frequency	8-bit tone fine adjustment							
R_1	01						4-bit tone fine adjustment			
R_2	02	Channel B frequency	8-bit tone fine adjustment							
R_3	03						4-bit tone fine adjustment			
R_4	04	Channel C frequency	8-bit tone fine adjustment							
R_5	05						4-bit tone fine adjustment			
R_6	06	Noise frequency				5-bit noise frequency				
R_7	07	Sets mixer and general ports	*Port "1"	*Port "0"	Noise C	Noise B	Noise A	Tone C	Tone B	Tone A
R_8	08	Channel A sound level				M	L_3	L_2	L_1	L_0
R_9	09	Channel B sound level				M	L_3	L_2	L_1	L_0
R_A	0A	Channel C sound level				M	L_3	L_2	L_1	L_0
R_B	0B	Envelope frequency	8-bit tone fine adjustment							
R_C	0C		8-bit coarse adjustment							
R_D	0D	Envelope form					CONT	ATT	ALT	HOLD
	0E	Data of input port	See the general port bit assignment table							
R_F	0F	Data of output port								

* Always keep the "port" bits of the register R7 at the levels shown above.

■ GENERAL PORTS

The input port has address 0E (H) and the output port 0F (H). They are controlled by an output port data latching register RF. The table at right shows relationships of bits and input/output terminals.

Relationships of bits and input/output terminals

Port	Bit	i/o	Connecting terminal name
Input	B_0	i	F WD1 or FWD2 (B6 of the output port selects FWD1 or FWD2. When B6 = "1", signal comes from FWD2.)
	B_1		BACK1 or BACK2
	B_2		LEFT1 or LEFT2
	B_3		RIGHT1 or RIGHT2
	B_4		TRGA1 or TRGA2
	B_5		TRGB1 or TRGB2
	B_6		JIS/50
	B_7		CMI
Output	B_0	o	TRGA1
	B_1		TRGB1
	B_2		TRGA2
	B_3		TRGB2
	B_4		STB1
	B_5		STB2
	B_6		Input select of input port B0 ~ B5 (not delivered to outside)
	B_7		$\overline{KANA}$

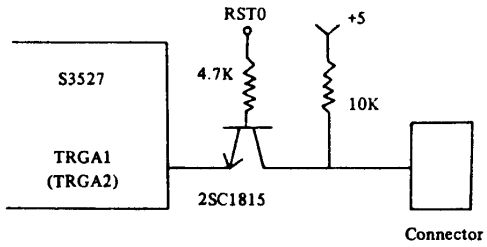
In initialized state, the terminals TRGA1, TRGB1, TRGA2, TRGB2 and STB2 are at "0" level; they go up to the prescribed level when the MSX BASIC is started. This being the case, the following explanation should be heeded when installing the MOUTH,which is to be connected to the general port. Attention is particularly necessary concerning the MSX MOUTH for setting the MOUTH mode at the time of turning on power supply.

In the initialization of the present device, mode A is selected in anticipation of any one of the above-indicated terminals going to "1" level. Mode B is selected by driving this level to "0" by operating a switch belonging to the MOUTH. Now, as mentioned above, no terminal goes to "1" level: this means that the MOUTH cannot be placed in mode A.

How to overcome this problematic situation follows:

- Connect the MOUTH when power supply is turned on for the MSX including the present device. If you already have the MOUTH connected before turning on power supply, disconnect it, turn on power supply and reconnect it. (The MOUTH will then automatically go into mode A.)
- By means of TRGA1 (TRGA2), set the mode of the MOUTH.
- Install such as a push-button switch in the power supply circuit from which the general port draws energy.

With the MOUTH installed as above, its mode can be set even when the MSX proper is in energized state (power supply ON). Such a MOUTH can be more conveniently made use of.

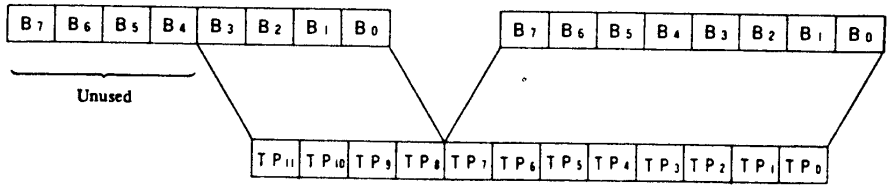


■ SETTING MUSIC SOUND FREQUENCIES (WITH REGISTERS $R_0 \sim R_5$)

Registers $R_0 \sim R_5$ define the frequencies of square waves which music sound generators of channels A, B, and C produce. R_0 and R_1 define frequency of channel A, R_2 and R_3 of channel B, R_4 and R_5 of channel C. The contents TP (decimal) of a register define frequency FT as follows. $F\phi$ is the clock frequency.

$$F_T = \frac{F\phi}{32TP}$$

Tone Coarse Adjustment Registers (R_1, R_3, R_5) Channels (A, B, C) Tone Fine Adjustment Registers (R_0, R_2, R_4)



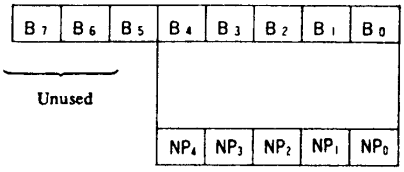
12-bit Value (TP) Defining Frequency

■ SETTING NOISE FREQUENCY (WITH REGISTER R_6)

The contents NP (decimal) of a register define the noise frequency FN as follows. $F\phi$ is the clock frequency.

$$F_N = \frac{F\phi}{32NP}$$

Noise Frequency Register R_6

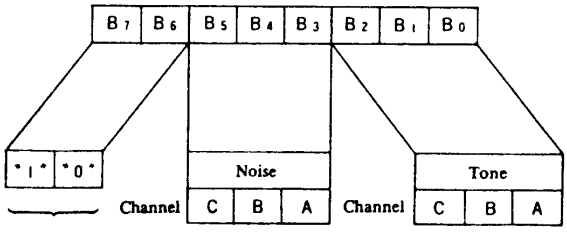


5-bit Value (NP) Defining Noise Frequency

■ SETTING THE MIXER (WITH REGISTER R_7)

The mixer mixes music sounds with noise according to bits $B_5 \sim B_0$ of register R_7. "0" denotes that sound or noise be produced while "1" not. If "0" is designated for both sound and noise, they will appear mixed. If "0" is designated for sound or noise alone, it will appear unmixed. If "1" is designated for both sound and noise, none will be produced.

Mixer Setting Register R_7

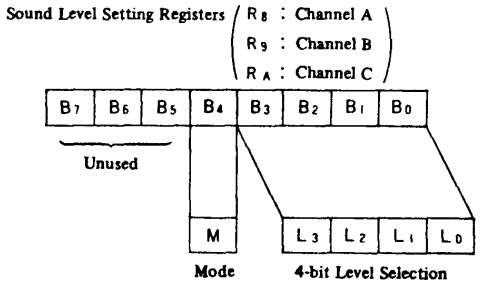


Always Set Just Like this

"0" Denotes that Sound or Noise be Produced

■ SOUND LEVEL CONTROL (WITH REGISTERS R_8 ~ R_A)

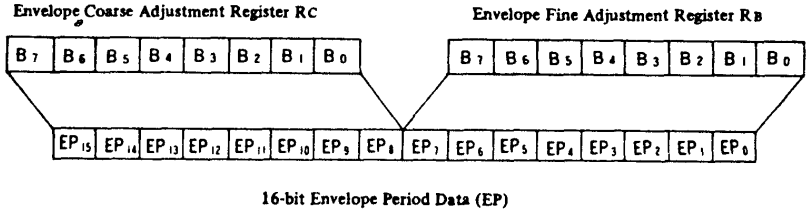
Registers R_8 ~ R_A control the sound levels of channels A, B, and C. M selects fixed sound level (M = 0) or variable level (M = 1). When M = 0, one of 16 levels will be selected with a 4-bit signal L_3 L_2 L_1 L_0. To change sound level, vary L_3 L_2 L_1 L_0. When M = 1, sound level is determined with a 5-bit signal E_4 E_3 E_2 E_1 E_0 the built-in envelope generator generates. E_4 E_3 E_2 E_1 E_0 varies with time.



■ SETTING ENVELOPE FREQUENCY (WITH REGISTERS R_B AND R_C)

The envelope period data EP (decimal) determines the envelope repetition frequency FE as follows. $F\phi$ is the clock frequency.

$$F_E = \frac{F\phi}{512EP}$$



■ ENVELOPE FORM CONTROL (WITH REGISTER RD)

The 5-bit signal E_4 E_3 E_2 E_1 E_0 of the built-in envelope generator determines the envelope level. The envelope form is determined by incrementing or decrementing a counter of the envelope generator, stopping it every cycle, or repeating to do such things. Bits B_3 ~ B_0 of register RD control the envelope form.

Envelope form control register RD

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
				CONT	ATT	ALT	HOLD

Envelope Form Control Signals

The envelope form varies as follows depending on CONT, ATT, ALT, and HOLD.

Envelope forms

B_3	B_2	B_1	B_0	Envelope form
CONT	ATT	ALT	HOLD	
0	0	×	×	
0	1	×	×	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

$1/f_1$ ← Envelope repetition period

■ D/A CONVERTER

The D/A converter produces output as shown below when the maximum amplitude is normalized to 1V. The logarithmic conversion provides a wide dynamic range and a natural feeling of attenuation.

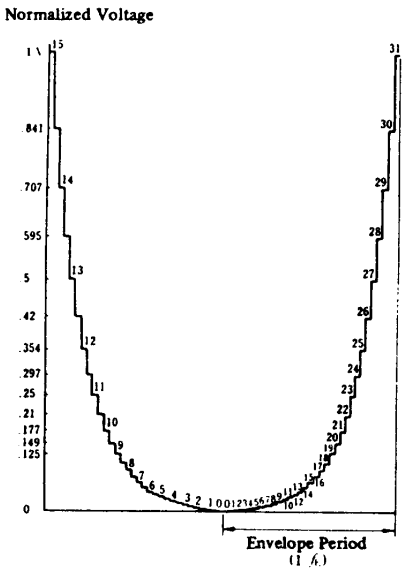


Figure 1 Output level of the D/A converter
The decimal values of sound level control signal L_3 L_2 L_1 L_0 are given along the left-side half of the curve and those of envelope counter output E_4 E_3 E_2 E_1 E_0 along the right-side half.

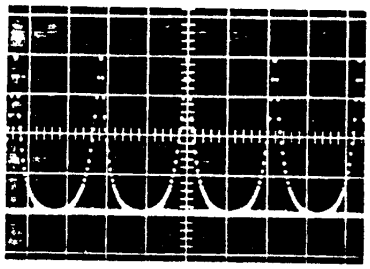


Figure 2 Waveform of a sound with envelope attached (R_D = × × × × 1110)

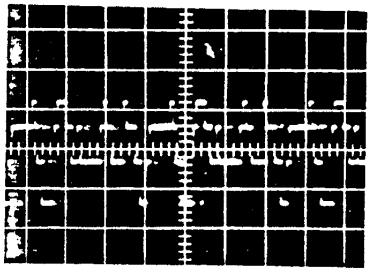
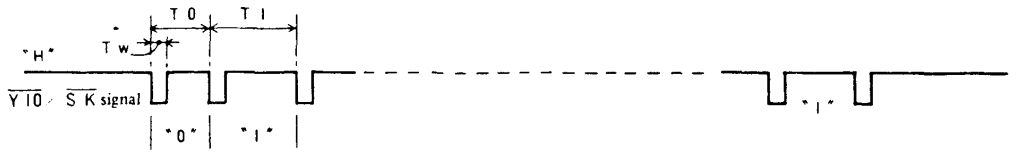


Figure 3 Waveform of three mixed sounds in fixed sound level (R_3 ~ R_1 = × × × 01100)

> Serial Key Input

If initialization has been performed to accept serial key input, serial data coming from the $\overline{Y10}$ / $\overline{SK}$ terminal according to the specifications given below can be ORed with key return signal.



B_{15}	B_{14}	B_{13}	B_{12}	B_{11}	B_{10}	B_9	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0

Figure 1 Output level of the D/A converter

Timing of serial signal

Symbol	MIN	MAX
T_w	$\frac{265}{F\phi}$	——
T_0	——	$\frac{2040}{F\phi}$
T_1	$\frac{2056}{F\phi}$	——
$T_0 - T_w$	$\frac{8}{F\phi}$	——

$F\phi$: Clock frequency

The serial signal coming to the $\overline{Y10}$ / $\overline{SK}$ terminal may be asynchronous to the clock. The waveform and timing should be as shown above. "0" is discriminated from "1" by the length of interval between negative pulses. In the above example, the input data are a series of "0", "1", . . . , "1" from left to right. The data enters a 16-bit register (B_{15} ~ B_0). If more input signal follows, it enters bit B_0 of the register with the contents of B_0 ~ B_{14} shifted to B_1 ~ B_{15} one bit each and the old content of B_{15} discarded.

After feeding in the serial input signal as above, set the contents ("Os" and "Is") of the keyboard drive register as shown in the bit allocation table, indicated below, which is for the keyboard and slot specifying register.

Select units of 8 bits each, as in the case of keyboard return signal, and read in the selected units to clear the 16-bit serial data register.

Reading serial data and clearing register

Keyboard drive bits		Description
B_0	B_1	
0	0	$B_0 \sim B_7$) Read from the same I/O address as of keyboard return signal.
0	1	$B_8 \sim B_{15}$) B_0 and B_8 correspond to X_0 of keyboard return.
1	X	Clears 16-bit register of serial data.

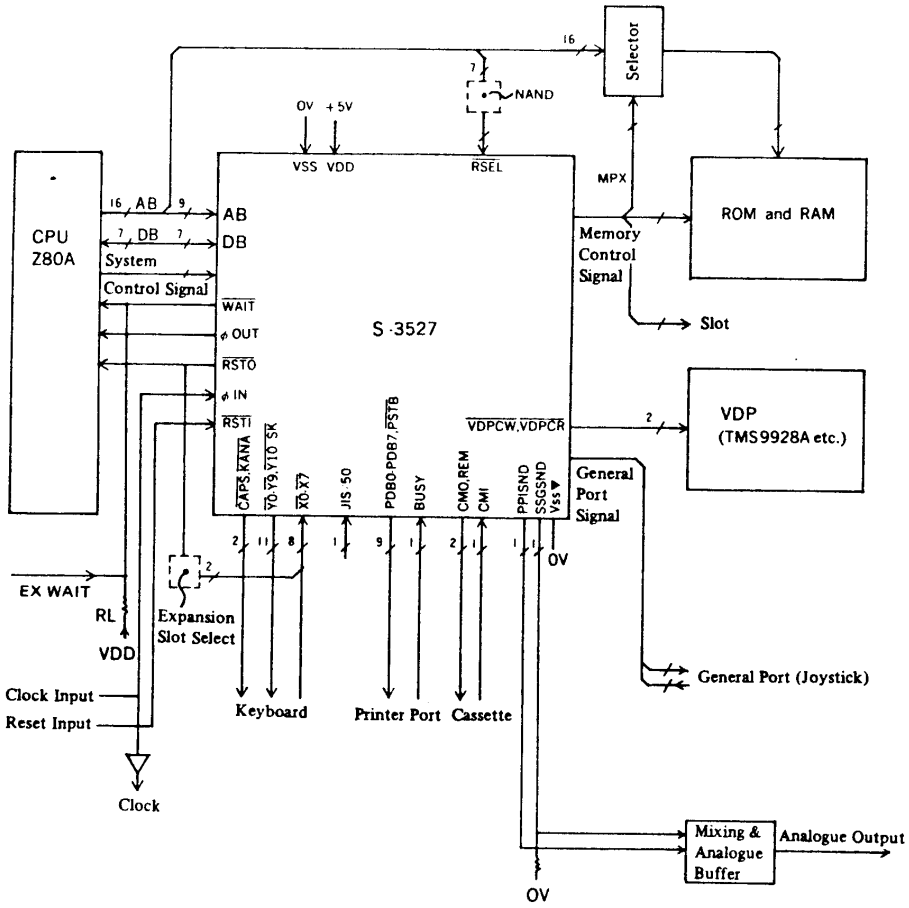
The 16-bit register will be cleared when B_0 is set to 1. By setting $B_1 \sim B_3$ appropriately, output can be delivered to any of the keyboard drive output terminals $\overline{Y_1}$, $\overline{Y_3}$, $\overline{Y_5}$, $\overline{Y_7}$, and $\overline{Y_9}$ just when the 16-bit register is cleared. The output signal can be sent out as the next serial data.

NOTES:

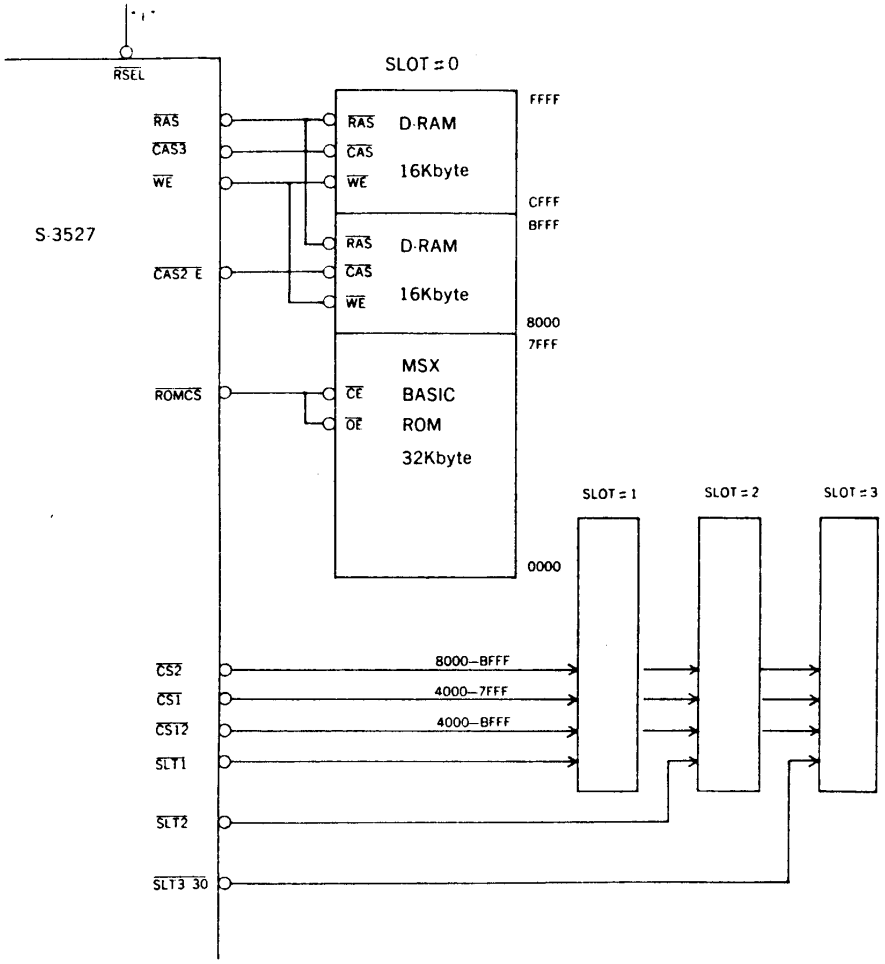
1) MSX does not support serial data.

2) If a serial data and a keyboard return signal come in to the CPU simultaneously, they will be ORed and read.

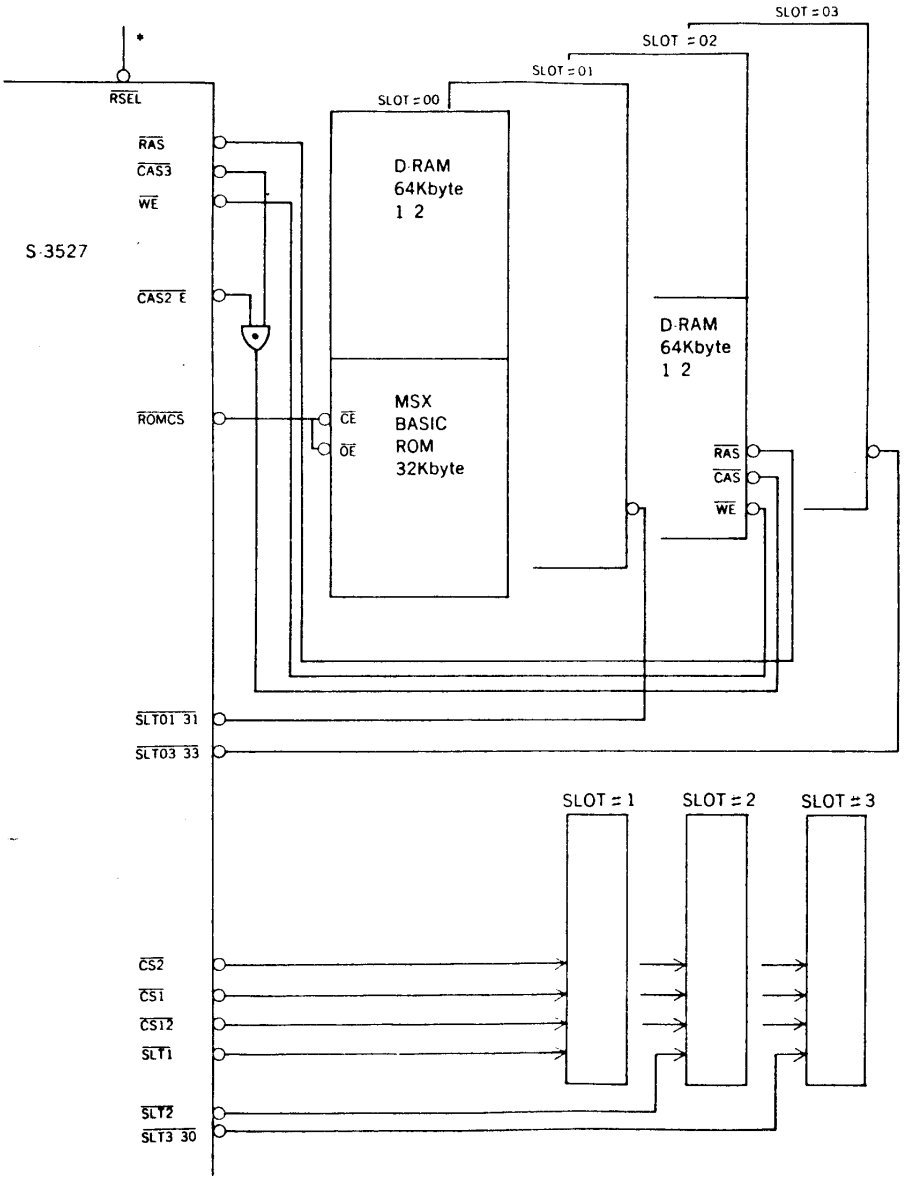
Sample basic circuit (S-3527 and peripheral devices)



Sample basic circuit (Memory control: expansion slot unused)

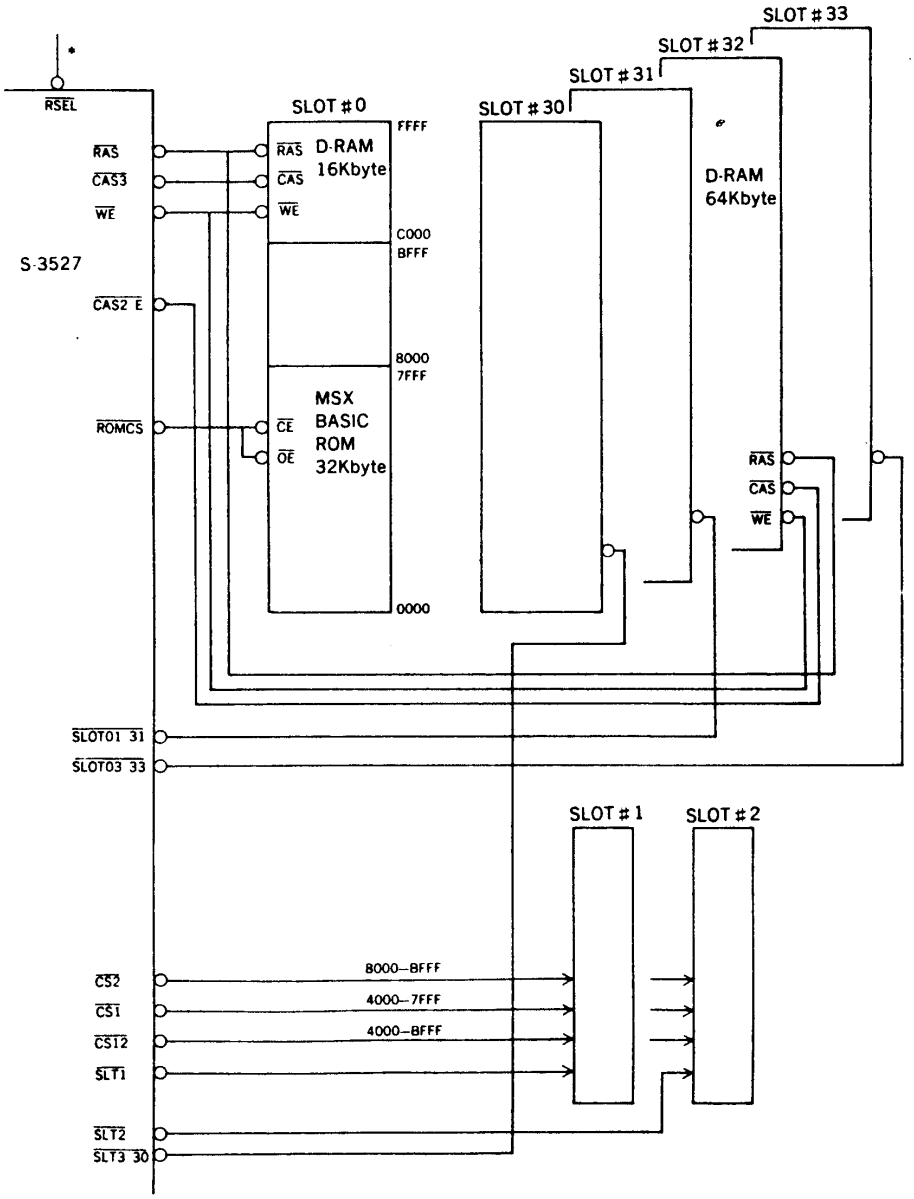


Sample basic circuit (Memory control: RAM 64 Kbyte: expansion slot # 0 used)



* The address bits which are not entered the S-3527 are NANDed and entered here.

Sample basic circuit (Memory control: RAM 16K + 64 Kbyte: expansion slot # 3 used)



* The address bits which are not entered the S-3527 are NANDed and entered here.

■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

Parameter	Rating	Unit
Supply voltage (VDD)	−0.3 ~ 7.0	V
Input terminal voltage	−0.3 ~ VDD + 0.3	V
Ambient temperature	0 ~ 70	°C
Storage temperature	−50 ~ 125	°C

2. Recommended operating conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply voltage	VDD	4.75	5.0	5.25	V
	VSS	0	0	0	V

3. DC characteristics (Top= 0°C~70°C, VDD=4.75v~5.25v, VSS=0V, VSS=0V)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Low input voltage	VIL1	(Except for $\overline{X_7} \sim \overline{X_0}$)	−0.3		0.8	V
	VIL2	($\overline{X_7} \sim \overline{X_0}$)	−0.3		1.5	V
High input voltage	VIH1	(Except for $\overline{X_7} \sim \overline{X_0}$)	2.0		VDD	V
	VIH2	($\overline{X_7} \sim \overline{X_0}$)	3.5		VDD	V
Low output voltage	VOL1	Note O): IOL = 10 mA ($\overline{PSTB}$, $\overline{WAIT}$, $\overline{CAPS}$, $\overline{KANA}$)	0		0.45	V
	VOL2	Note O): IOH = 0.2 mA	0		0.45	V
High output voltage	VOH		4.0		VDD	V
Input current	II	VIN = 0V	−50		−500	μA
Input leakage current	ILI	VIN = 0 ~ 5V			10	μA
Output leakage current	ILO	VO = 0 ~ 5V			10	μA
Supply current	IDD				35	mA

Note O) : IOL = 1mA CMO, REM, PPiSND, $\overline{VDPCR}$, $\overline{VDPCW}$, φOUT, $\overline{ROMCS}$, $\overline{RAS}$, $\overline{CAS3}$, $\overline{CAS2/E}$, $\overline{WE}$, $\overline{TRGA1}$, $\overline{TRGB1}$, $\overline{STB1}$ TRGA2, TRGB2, STB2, $\overline{Y10/SK}$, $\overline{Y0}$~$\overline{Y9}$

IOL = 2.4mA ($\overline{DB0}$~$\overline{DB7}$, $\overline{SLT01/31}$, $\overline{SLT03/33}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS12}$, $\overline{SLT2}$, $\overline{SLT3/30}$, PDB0~PDB7, $\overline{RST0}$, MPX)

IOL = 1.6mA ($\overline{TRGA1}$, $\overline{TRGA2}$, $\overline{STB1}$, $\overline{TRGA2}$, $\overline{TRGB2}$, $\overline{STB2}$) ..... Max. VOL = 0.5V

IOH = 0.2mA DB0 ~ DB7, $\overline{ROMCS}$, MPX, $\overline{RAS}$, $\overline{CAS2/E}$, $\overline{CAS3}$, $\overline{WE}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS12}$, $\overline{SLT1}$, $\overline{SLT2}$, $\overline{SLT3/30}$, $\overline{SLT01/31}$, $\overline{SLT03/33}$, $\overline{VDPCR}$, $\overline{VDPCW}$, PDB0 ~ PDB7, $\overline{PSTB}$, CMO, REM, $\overline{RSTO}$, PPiSND, STB1, STB2

4. AC Characteristics (See Note 1.)

Clock timing

Parameter	Symbol	Condition	Min.	Typical	Max.	Unit
Clock period	T_C			280		ns
Rise/decay times of clock (input)	$T_{\phi Ir}, T_{\phi If}$				30	ns
Delay time of clock (input/output)	$T_{\phi I, \phi O}$			13		ns
Rise/decay times of clock (output)	$T_{\phi or}, T_{\phi of}$	C_L = 70PF			30	ns

Write timing

Parameter	Symbol	Condition	Min.	Max.	Unit
Data stable before $\overline{WR}$	T_{WRS}		300		ns
Data valid after $\overline{WR}$	T_{WRH}		0		ns
Output data delay	T_{DD}	Note 2)		250	ns

Read timing

Parameter	Symbol	Condition	Min.	Max.	Unit
Data delay	$T_{\overline{RDD}}$			250	ns
Time to data floating	T_{RDF}			100	ns
Data stable before $\overline{RD}$	$T_{\overline{RDS}}$	Note 3)	0		ns
Data valid after $\overline{RD}$	T_{RDH}		0		ns

Notes:

1) The address and data buses and control signal lines are assumed to be connected directly to the CPU.

2) Applies to $\overline{Y_0}$ ~ $\overline{Y_{10}}$, STBI, STB, TRGAI, TRGA2, TRGBI, TRGB2, $\overline{CAPS}$, $\overline{KANA}$, REM, and CMO.

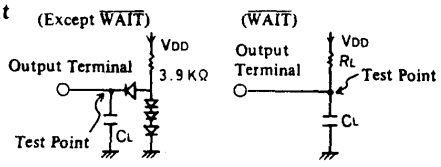
3) Applies to $\overline{X_0}$ ~ $\overline{X_7}$, FWD1, FWD2, BACK1, BACK2, LEFT1, LEFT2, RIGHT1, RIGHT2, TRGA1, TRGA2, TRGB1, TRGB2, CMI, and JIS/50.

M1 cycle, memory read/write cycle, and I/O cycle timing

Parameter	Symbol	Condition	Min.	Max.	Unit
CLOCK ↑ – $\overline{WAIT}$ ↓ Delay time	$T_{\phi\overline{WA}}$	C_L = 70PF		60	ns
CLOCK ↑ $\overline{WAIT}$ ↑ "	$T_{\phi WA}$	C_L = 70PF R_L = 680Ω		60	ns
$\overline{MREQ}$ ↓ – $\overline{RAS}$ ↓ "	$T_{\overline{MRRA}}$	C_L = 100PF		60	ns
$\overline{MREQ}$ ↑ – $\overline{RAS}$ ↑ "	T_{MRRA}	"		70	ns
CLOCK ↑ – $\overline{RAS}$ ↓ "	$T_{\phi\overline{RA}}$	"		70	ns
$\overline{CLOCK}$ ↑ – $\overline{RAS}$ ↑ "	$T_{\overline{\phi}RA}$	"	90	180	ns
CLOCK ↑ – MPX ↑ "	$T_{\phi MX}$	"		70	ns
$\overline{MREQ}$ ↑ – MPX ↓ "	$T_{MR\overline{MX}}$	"		70	ns
$\overline{RAS}$ ↓ – MPX ↑ "	$T_{\overline{RA}MX}$	"	50		ns
$\overline{CLOCK}$ ↑ –*$\overline{CASn}$ ↓ "	$T_{\overline{\phi}\overline{CA}}$	"		70	ns
$\overline{MREQ}$ ↑ –*$\overline{CASn}$ ↑ "	T_{MRCA}	"		70	ns
CLOCK ↑ – $\overline{WE}$ ↑ "	$T_{\phi WE}$	"	30	70	ns
CLOCK ↑ – $\overline{WE}$ ↓ "	$T_{\phi\overline{WE}}$	"	30	70	ns
$\overline{MREQ}$ ↓ – $\overline{ROMCS}$ ↓ "	$T_{\overline{MRRO}}$	"		70	ns
$\overline{MREQ}$ ↑ – $\overline{ROMCS}$ ↑ "	T_{MRRO}	"		70	ns
$\overline{MREQ}$ ↓ –*$\overline{CSn}$ ↓ "	$T_{\overline{MRCS}}$	"		60	ns
$\overline{MREQ}$ ↑ –*$\overline{CSn}$ ↑ "	T_{MRCS}	"		70	ns
$\overline{MREQ}$ ↓ – $\overline{SLTn}$ ↓ "	$T_{\overline{MRSL}}$	"		60	ns
$\overline{MREQ}$ ↑ –*$\overline{SLTn}$ ↑ "	T_{MRSL}	"		70	ns
$\overline{MREQ}$ ↓ –*$\overline{SLTnn}$ ↓ "	$T_{\overline{MRST}}$	"		70	ns
$\overline{MREQ}$ ↑ –*$\overline{SLTnn}$ ↑ "	T_{MRST}	"		70	ns
$\overline{RD}$ ↓ – $\overline{VDPCR}$ ↓ "	$T_{\overline{RD}\overline{VR}}$	"		70	ns
$\overline{RD}$ ↑ – $\overline{VDPCR}$ ↑ "	T_{RDVR}	"		70	ns
$\overline{WR}$ ↓ – $\overline{VDPCW}$ ↓ "	$T_{\overline{WR}\overline{VW}}$	"		70	ns
$\overline{WR}$ ↑ – $\overline{VDPCW}$ ↑ "	T_{WRVW}	"		50	ns

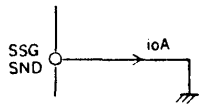
* : See Note 4)

Load of timing test circuit

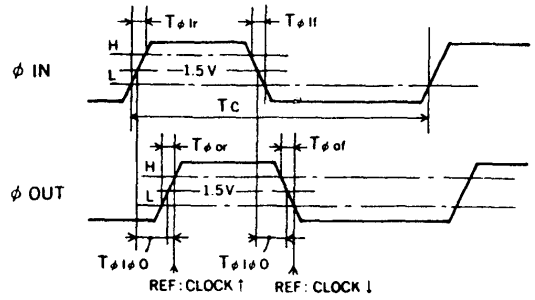


Analog output (SSG SND)

Parameter	Symbol	Condition	Min.	Typical	Max.	Unit
Maximum output current	I_{OA}	See below	(0.8)	(1.2)	1.7	mA_{PP}

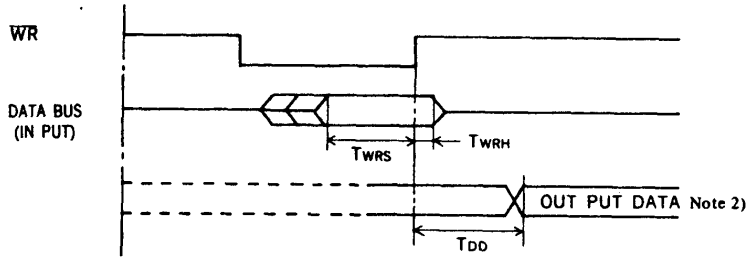


Clock timing

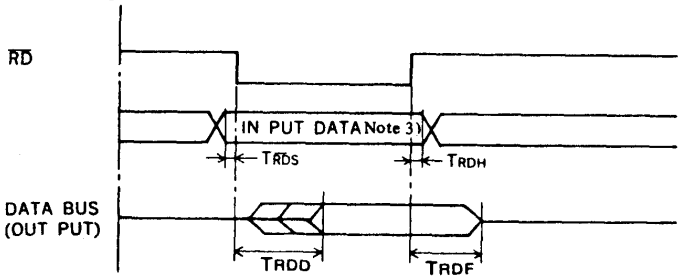


	"H"	"L"
CLOCK(φ OUT)	V_{DD}–0.6V	0.45V
OUT PUT	2.0V	0.8V
IN PUT or φ IN	2.0V	0.8V
FLOAT	ΔV	±0.5V

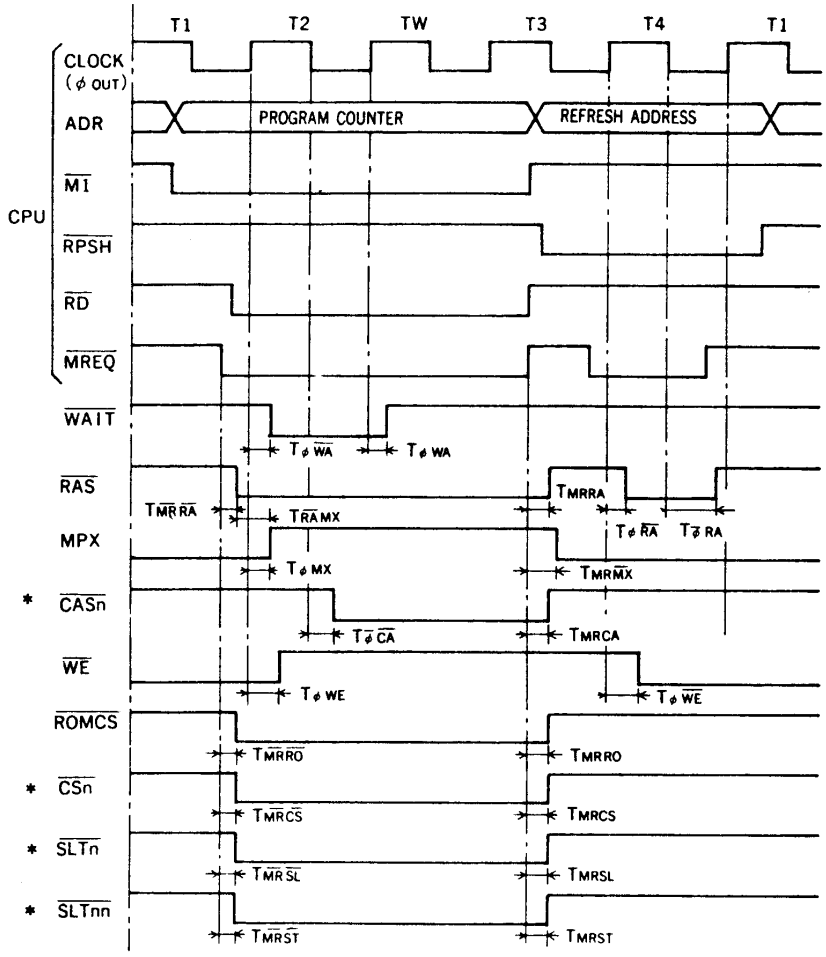
Write timing



Read timing



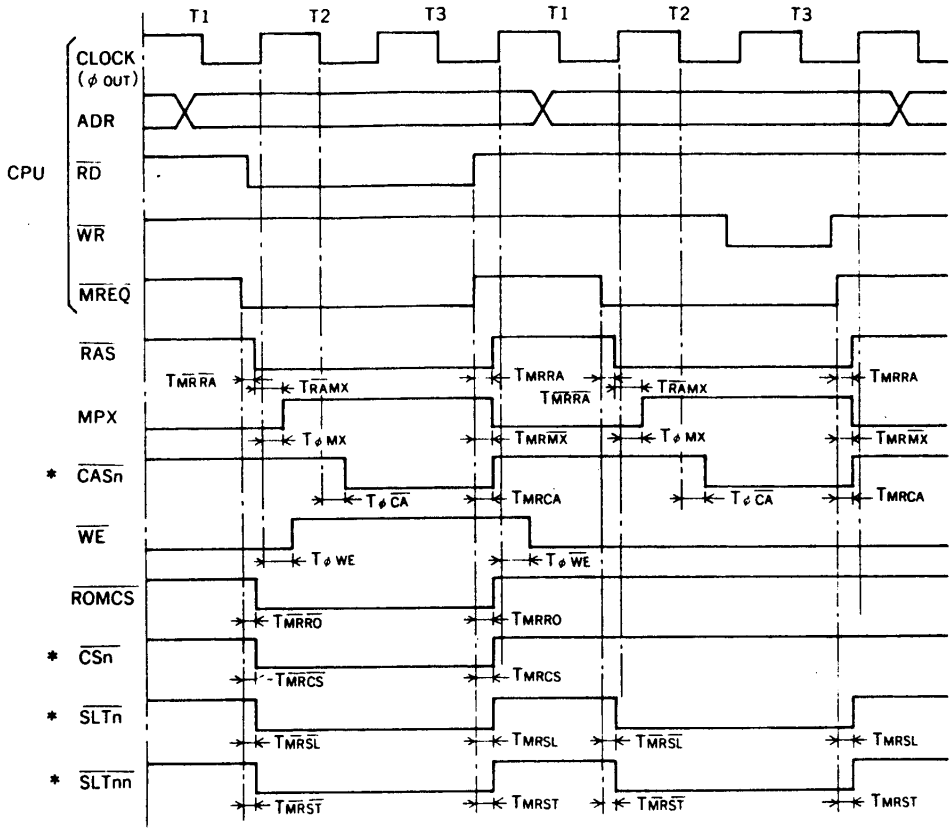
M1 cycle timing



Note 4) : The signal names marked with * are detailed below.

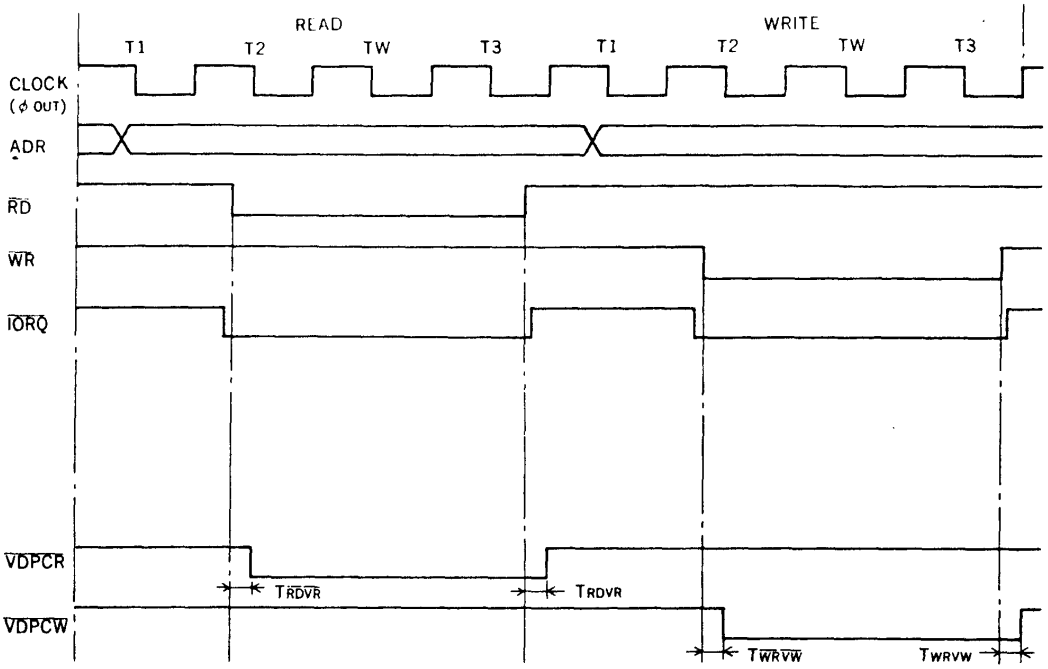
CASn	: CAS 2/E, CAS 3
CSn	: CS1, CS 2, CS12
SLTn	: SLT1, SLT 2, SLT 3/30
SLTnn	: SLT01/31, SLT03/33

Memory read/write timing

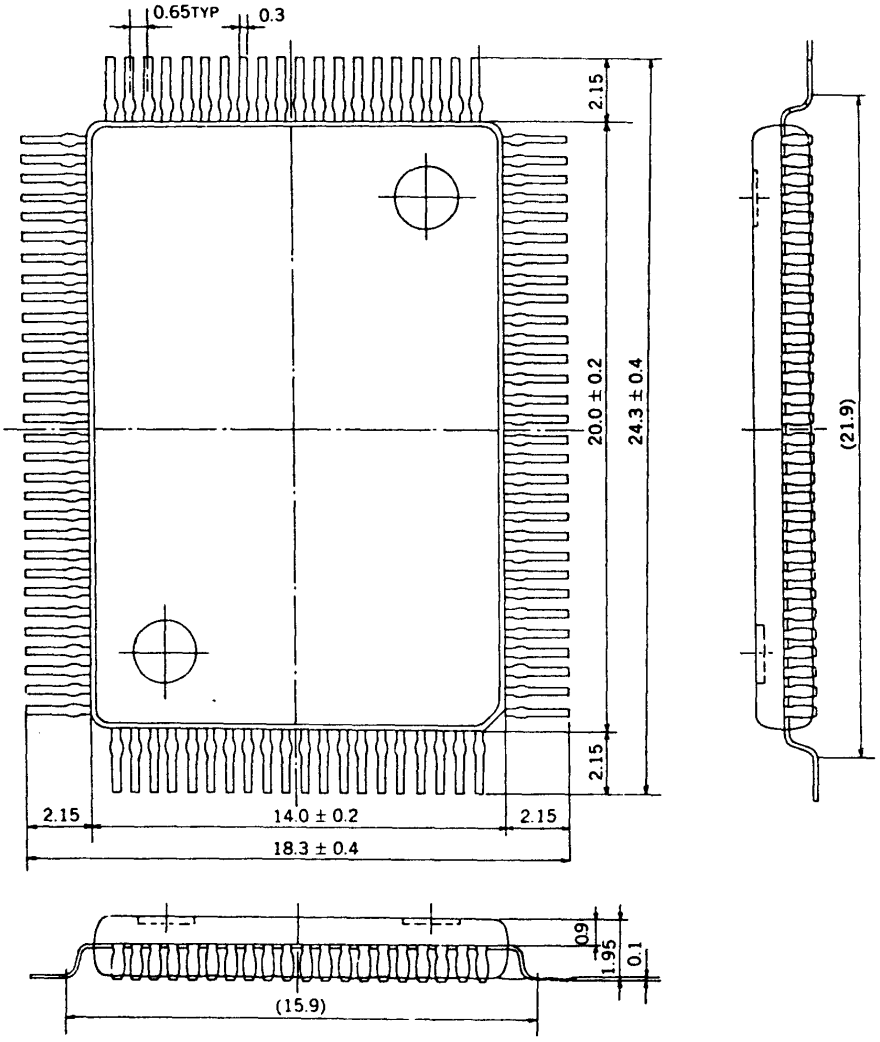


* : See Note 4)

I/O cycle timing



■ EXTERNAL DIMENSIONS DIAGRAM



> Precautions for Use

The S-3527 is a CMOS device and its input terminals will be directly connected to the outside. When using it, protect it from latch-up and static electricity.

Latch-up is likely to happen in the following cases.

- A signal line is connected to the S-3527 from a separate system to which power is supplied separately from the S-3527, and the S-3527's power is later to rise than the other's.
- A surge voltage rises when power has turned on.
- The supply voltage of the S-3527 exceeds the rated range.
- The resistance of the power lines connected to the S-3527 is not low.
- A separate system has been connected to an input/output terminal while the S-3527 is operating.
- Someone has touched an input/output terminal by part of his body like hand while the S-3527 is operating.