PROCYON ARCADE FPGA HDMI

BOARD BRIEF DESCRIPTION

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Procyon copyright ownership announcement and statement:
This announcement is entered into by Maxim Vlasov, the sole inventor and creator of Procyon system architecture and design. Procyon IP family is wholly created on the Maxim Vlasov's own time with the assistance of the personally owned resources, including all design equipment and scientific instruments, without any participation of any other contributors or sponsors.

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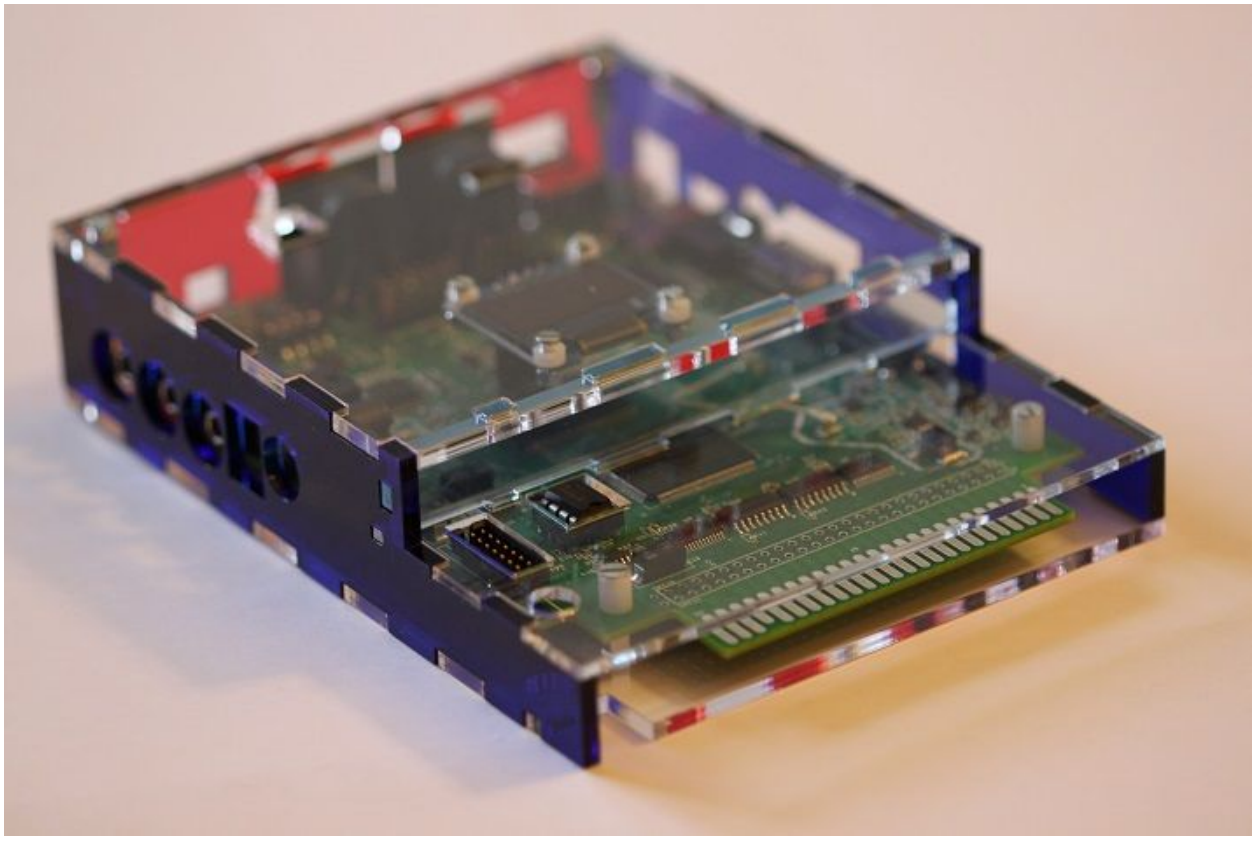
Revision History

Revision	Release Date	Remarks
0.1	May the 5th 2016	Initial release
1.0	October the 2nd 2016	Released to public
1.1	October the 30th 2016	Minor update



Introduction

Procyon-Arcade (shortly Procyon) is the FPGA based multimedia board designed to accurately emulate the architecture of the classic 8 bit and 16 bit computers of the 80s era.
The card opens up the new user experience paradigm by using all around modern interconnect with your digital home entertainment system.
The vast majority of the home computers of 80s were designed for the TV monitor connectivity and mono audio. 15 KHz monitors became obsolete already in 90s and now days are very rare.
Procyon board provides the cycle accurate VDP (Video Display Processor) emulation with the seamless connectivity to the modern HDTV or PC monitor via HDMI or DVI-D link.
This solution has no time lag and no visible noise and image aliasing artifacts typical for the VIDEO to VGA/HDMI converters.
The audio is generated internally by the cycle accurate PSG (Programmable Sound Generator) and SCC (Sound Creative Chip) IP models and distributed via the HI-FI analog audio chain and the digital optical link TOSLINK (Toshiba optical fiber digital interface).
This board can be either a seamless add-on to the existing 8 bit computer architecture or can also accurately emulate the classic computers including MSX, Commodore C64 and many others.

Also this board can be used in many applications as the multimedia extension, including mobile robotics, industrial, home automation etc.

Procyon Operating Modes

Procyon can be used either as:

- independent self-contained FPGA based System On a Chip with enhanced multimedia capabilities
- add-on audio-visual and storage controller
- stacked-up distributed computing system

Board can run either solely or in a stack together with the identical boards. The mezzanine connectors provide the robust high speed interconnect between the stacked Procyon-Arcade systems.

Nevertheless, the main goal for Procyon-Arcade was the compatibility with the MSX computer system architecture. In that context, Procyon board can operate in two main modes:

- MSX multimedia expansion;
- Stand-alone microcomputer emulation.

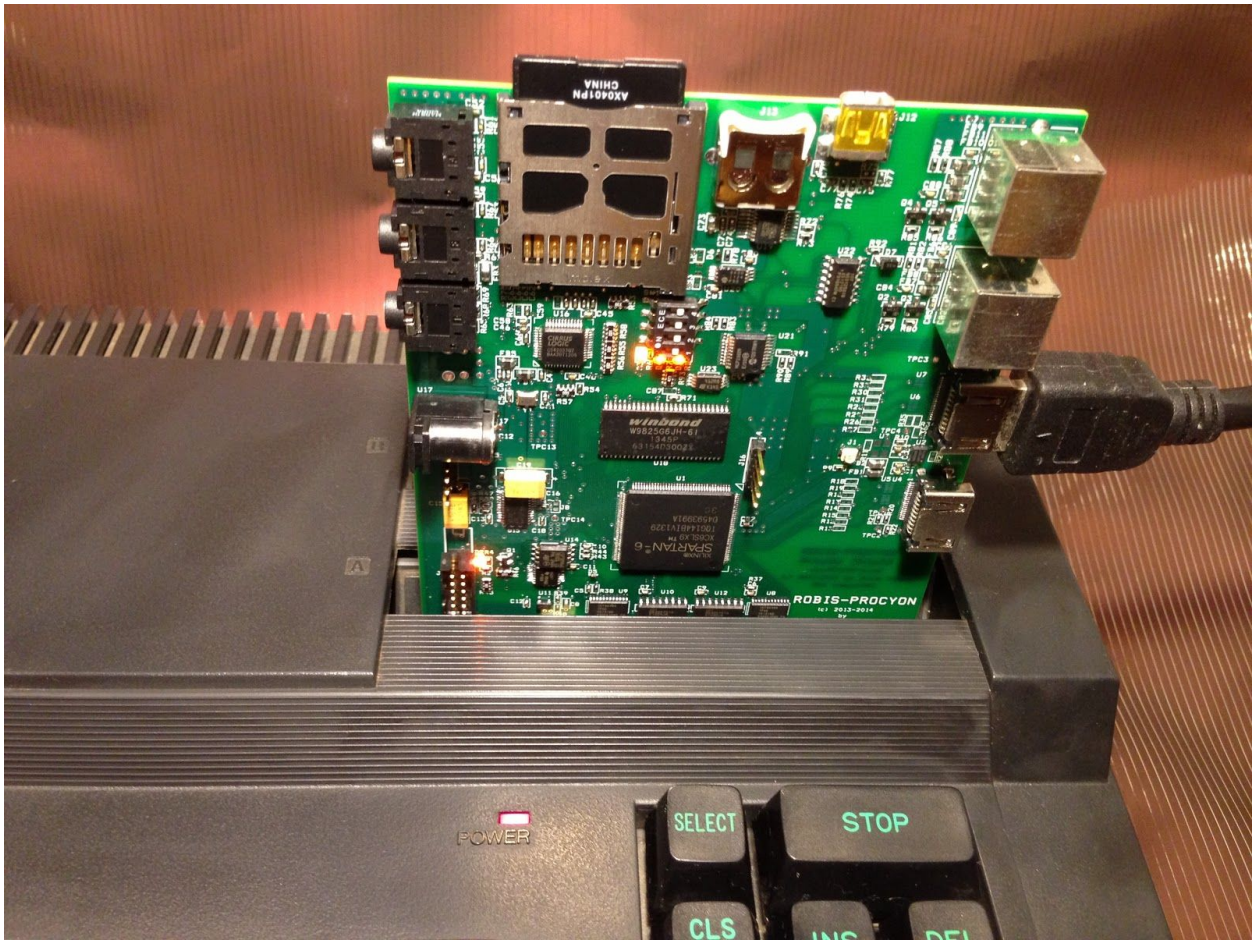
In the MSX multimedia expansion mode, the board replicates the MSX screen over the HDMI interface on the HDTV or modern flat screen monitor.

In the stand-alone mode the board can incorporate all the crucial computer IP modules and provide the accurate real-time emulation with the video output via the HDMI interface.

The board has a very rich audio emulation and audio interconnect capabilities. Procyon emulates the standard popular microcomputer audio facilities and some famous synthesizers including the PSG AY8910, Konami SCC and SCC+ chips and Yamaha YM2413 music IC. The audio is digitally mixed and output via the analog line and headphone outputs and also via the digital SPDIF/TOSLINK interface and HDMI.

Use Case Scenario 1: Add-on Board

In this mode, Procyon is placed in the free MSX slot.
The MSX video output is replicated via the HDMI connection.
The audio is reproduced via the high definition audio link. The stereo audio input is internally digitized and mixed with the emulated PSG, SCC and PPI digital audio outputs. The mixing result is sent to the analog audio outputs (line out and headphones) and also the digital audio link SPDIF/TOSLINK.



The screen replication is performed in a seamless manner, where the external VDP core is running simultaneously with the original built-in MSX VDP. Both VDPs operate coherently. In other words, both VDPs operate under precisely equivalent conditions in time:

- Main system clock and start event (system reset);
- CPU access commands, data and events (interrupts);

Not all the required internal MSX signals are present on the slot connector. Hence, the synchronization between the internal VDP and Procyon is achieved indirectly by the means of the MSX master clock regeneration.

This method requires the computer video sync output (either from RGB connector or from the video output) and the precise phase locked loop (PLL) hardware. The latter generates the synchronization signal coherent to the internally available system clock of 21.477 MHz.
All the MSX/MSX2/MSX2+/MSX TurboR software will run natively without any additional driver support and produce the image via the HDMI video interface.
When MSX computers were manufactured with the factory fixed frame rate (50 or 60Hz), with an introduction of MSX2 and later platforms, the frame rate became programmable.
Many European game titles change the frame rate at the run-time multiple times.
Procyon receives the video or sync signal from the host MSX computer and continuously analyses it.
Once Procyon card detects the frame rate change, it changes its HDMI output format accordingly.
In the current implementation only 2 basic video modes are supported. All the 60Hz interlaced and progressive screen modes are mapped onto the standard VGA 640x480@60Hz progressive mode.
All the 50Hz interlaced and progressive modes are mapped onto the standard PAL 4:3 768x576@50Hz.
This way both type of the video display devices can be connected to Procyon card:

- DVI-D monitors and presentation projectors(via passive low cost HDMI->DVI-D adapter);
- HDMI HDTV and home video projectors

Vast majority of PC DVI-D monitors doesn't officially support 50Hz modes according to their specifications. Hence, the EDID (Extended Display Identification Data) is not consulted when the monitor is connected. Nevertheless, almost all the monitors do support unofficially and display the 50Hz modes (same chipsets are used for both PC monitors and the HDTVs).
On every screen mode change, within 10us FPGA emulated VDP switches to the new scan rate, however, the HDMI display backend takes about 2 second to complete the mode change. Therefore the screen blanking for about 2 seconds on every mode change is absolutely normal.
The maximum HDMI cable length is limited to 15 meters. Working with the loads farther than 15 meters require the active HDMI repeater.

On one hand, the digital audio is not running from the video synced PLL in order to suppress all the artifacts (flutter) on the PLL lock events. On the other, the digital audio doesn't use the MSX slot CPU clock due to the aftermarket turbo implementations, where the MSX slot timing spec is violated (clock runs much faster than 3.57 MHz).
The digital audio time base runs from the dedicated 24.576 MHz clock oscillator located in the HI-FI digital audio 20 bit ADC/DAC front-end IC. The clock is then regenerated and the 3.579545 MHz time reference is utilized by all the FPGA emulated audio sources. In the current implementation MSX PSG, PPI and Konami SCC are implemented and digitally mixed with the digitized analog stereo input. This analog stereo input can be connected to the external sources or to non-emulated sound generators like Yamaha SFG01, Yamaha SFG05 or many others.
The digital stereo mix is then serialized and sent via the optical TOSLINK digital interface via the

fiber optics or converted back by the D/A converter at 48 KSamples/s into the analog form and sent to the line out and amplified headphone socket.
Since the digital audio mix is generated at the 3.579545 MHz clock rate, its bandwidth must be limited before hand. This is done by the sample rate converter hardware implemented in the FPGA. The incoming audio samples are low pass filtered first, then decimated and finally come thru the antialiasing filter. The frequency band is limited to 18 KHz with the steep roll-off of 24dB above that frequency.
By using this technique the perceptive sound quality is very close to the original without having hum, noise and artifacts.

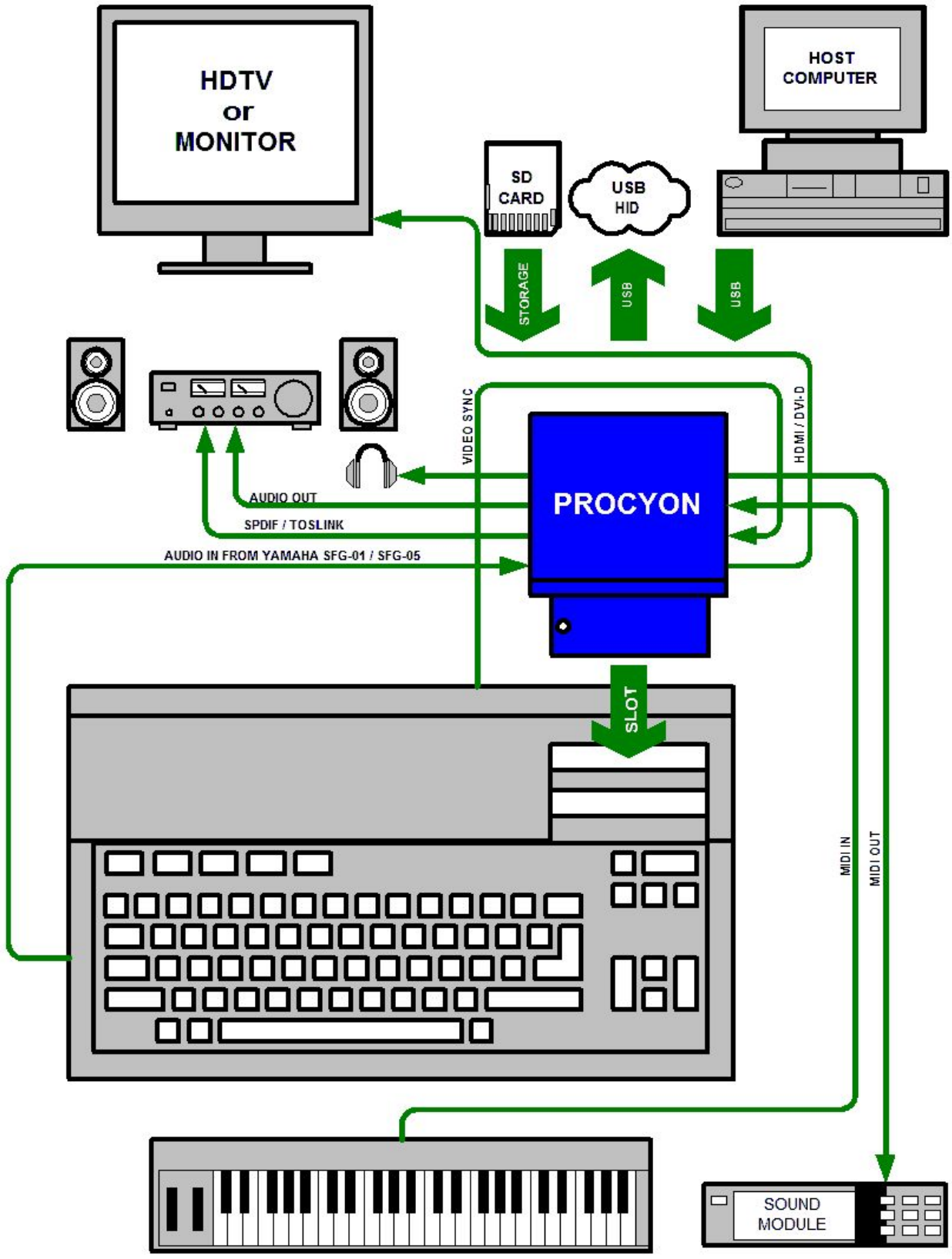
Also Procyon is equipped with MIDI I/O and emulates both the MSX AUDIO and MSX TurboR MIDI HW. MSX AUDIO MIDI HW is based on the ACIA (MC6850 from Motorola) IC, when the MSX TurboR MIDI HW is based on a different serial controller - USART (I8251 from Intel). Both peripherals are I/O mapped. The user can enable/disable the emulated hardware in the Procyon configuration menu. By default, the hardware is disabled to avoid the bus contention (HW conflict).

SD or SDHC card is utilized as the storage medium. Either MSX-DOS or MSX-DOS2 can be loaded from the Procyon configuration ROM at a boot-up time.
It is recommended to use MSX-DOS for the standard MSX computers and MSX-DOS2 for the MSX2 and beyond models. MSX-DOS2 requires both the memory extension and the DOS2 ROM subslots enabled simultaneously. Thus, MSX-DOS2 can only operate when Procyon is plugged into the non-expanded slot.

The board internal memory is present in the memory mapped sub-slot as the 4096 KBytes main RAM expansion. If Procyon resides in the slot number X, then the RAM expansion can be found in the subslot X.0.

Also there are 2 different USB type ports installed on the system. In the upstream mode the USB port connects the board to the USB host computer. Via this connection, the files and DFU (Device Firmware Upgrade) images can be copied onto the local storage medium (SD-CARD) and built-in FLASH ROM.
The downstream mode the USB port implements the full speed HID compatible host for the modern mouse and keyboard connection. The USB mouse and keyboard, however, require a special resident driver being installed in the MSX memory workspace. This is done automatically at the boot time. Nevertheless, some SW titles can’t use this extension since they don’t use MSX BIOS functions to access to the keyboard and/or mouse.

In the described above case, Procyon board runs in parallel to the built-in MSX computer hardware without up-stepping neither VDP version nor the MSX model. This is how 100% MSX/MSX2/MSX2+ and TurboR software can sound and display via Procyon audio/visual interface.


HDTV
or
MONITOR
HOST
COMPUTER
SD
CARD
USB
HID
STORAGE
USB
USB
VIDEO SYNC
HDMI / DVI-D
PROCYON
AUDIO OUT
SPDIF / TOSLINK
AUDIO IN FROM YAMAHA SFG-01 / SFG-05
SLOT
MIDI IN
MIDI OUT
SOUND
MODULE

However, there is another setup possible, where the existing MSX (MSX1) computer will be upgraded to MSX2/2+ model by Procyon emulated hardware.
In this case, the Procyon VDP no longer resides on the standard VDP MSX ports (0x98-0x9B), but occupies a different space (0x88-0x8B). MSX BIOS initialization is intercepted and the modified MSX2 ROM and SUBROM are pushed into the slot address space. In the following configuration, the modified MSX2 ROM announces that the new VDP (actually emulated VDPII Yamaha V9958) resides on the new HW ports (not conflicting with the original MSX VDP).
Most commercial titles released before 1989 do read the VDP port address information and use correctly the Procyon emulated VDP. Also all the other MSX2 facilities are properly emulated. This includes the RTC (Real-Time Clock) and also the RAM with the memory mapper.
By using the aforementioned technique, good proportion of the MSX2 software can run on the native MSX computer without any known issues.

The detailed low level operation in the add-on card mode is described in the HW chapters.

Use Case Scenario 2: Stand-alone Emulation

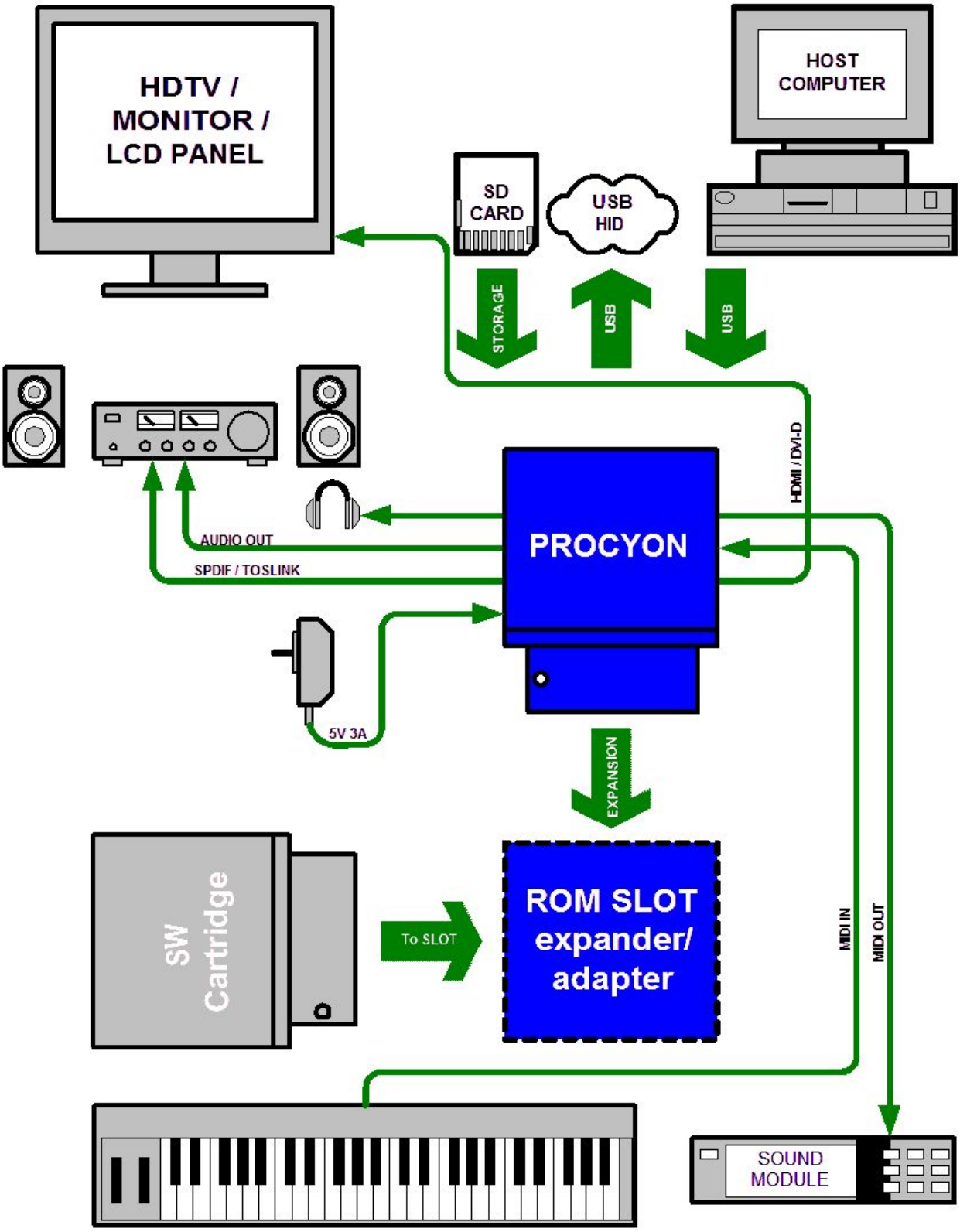
Procyon can also run in the stand-alone emulation mode.
Due to the limited resource capacity the on-board Xilinx FPGA can emulate a very light microcomputer architecture including popular home computers from 80s.
The external slots can be connected via a small adapter, which de-multiplexes the FPGA bus and routes dedicated slot select signals for the slots. Up to 3 unexpanded or 12 fully expanded slots can be supported externally.

Also, due to the robust high speed reconfigurable bus (which also acts as the slot connector), multiple Procyon cards can be combined to emulate more complex systems.

In one of the possible setups the graphics generated by one card can be passed through another Procyon card with the superimposed additional graphic features. This way many arcade computers and more complex architectures can be successfully emulated without any compromises on the video quality.

On the diagram below, the typical simple stand-alone setup is depicted. The card is powered by the external power adapter providing 5V DC. If standard cartridges to be used, a small slot adapter-demultiplexer needs to be connected between Procyon bus and the slot connectors. Also the same adapter will generate +/-12V necessary for the slot operation.

The external keyboard and the mouse are to be connected to the USB host ports.
Also Procyon has an upstream (device) port for the host computer connection. Like in the add-on setup, the host computer can upload/download files from the SD card, update the DFU images.


HDTV /
MONITOR /
LCD PANEL
HOST
COMPUTER
SD
CARD
USB
HID
STORAGE
USB
USB
HDMI / DVI-D
AUDIO OUT
SPDIF / TOSLINK
PROCYON
5V 3A
EXPANSION
SW
Cartridge
To SLOT
ROM SLOT
expander/
adapter
MDI IN
MIDI OUT
SOUND
MODULE

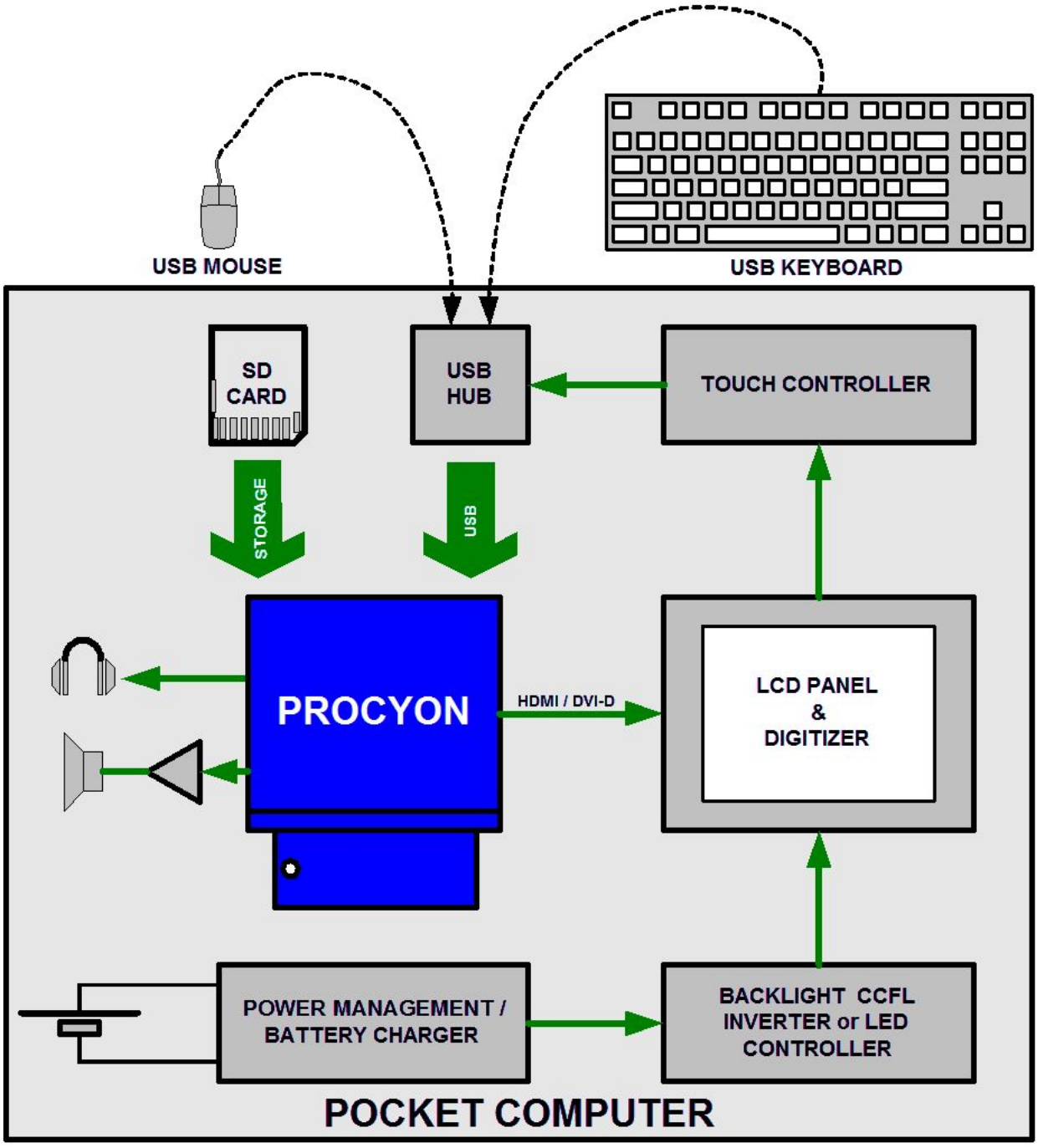
Besides, a very minimalistic setup is also possible by adding a simple power management system, LCD panel with built-in digitizer, backlight controller, touch controller and the loudspeaker amplifier circuit.

In the stand-alone mode, the all the internal HW runs from the built-in clock reference. No complex synchronization like in the add-on mode is required.

Nevertheless, the small size of Procyon permits building the pocket-size 8 or 16 bit computer. The modern displays with the screen sizes beyond 7” now are equipped with the same TMDS (HDMI or DVI-D) interface. I.e. any LCD panel can be easily integrated into the stand-alone setup.

In other words, by adding the power source, small power management board and the LCD panel, Procyon can be turned into the hand-held computer HW emulator.
In the same manner many other 8/16 bit computers and gaming consoles of 80s era can be emulated.

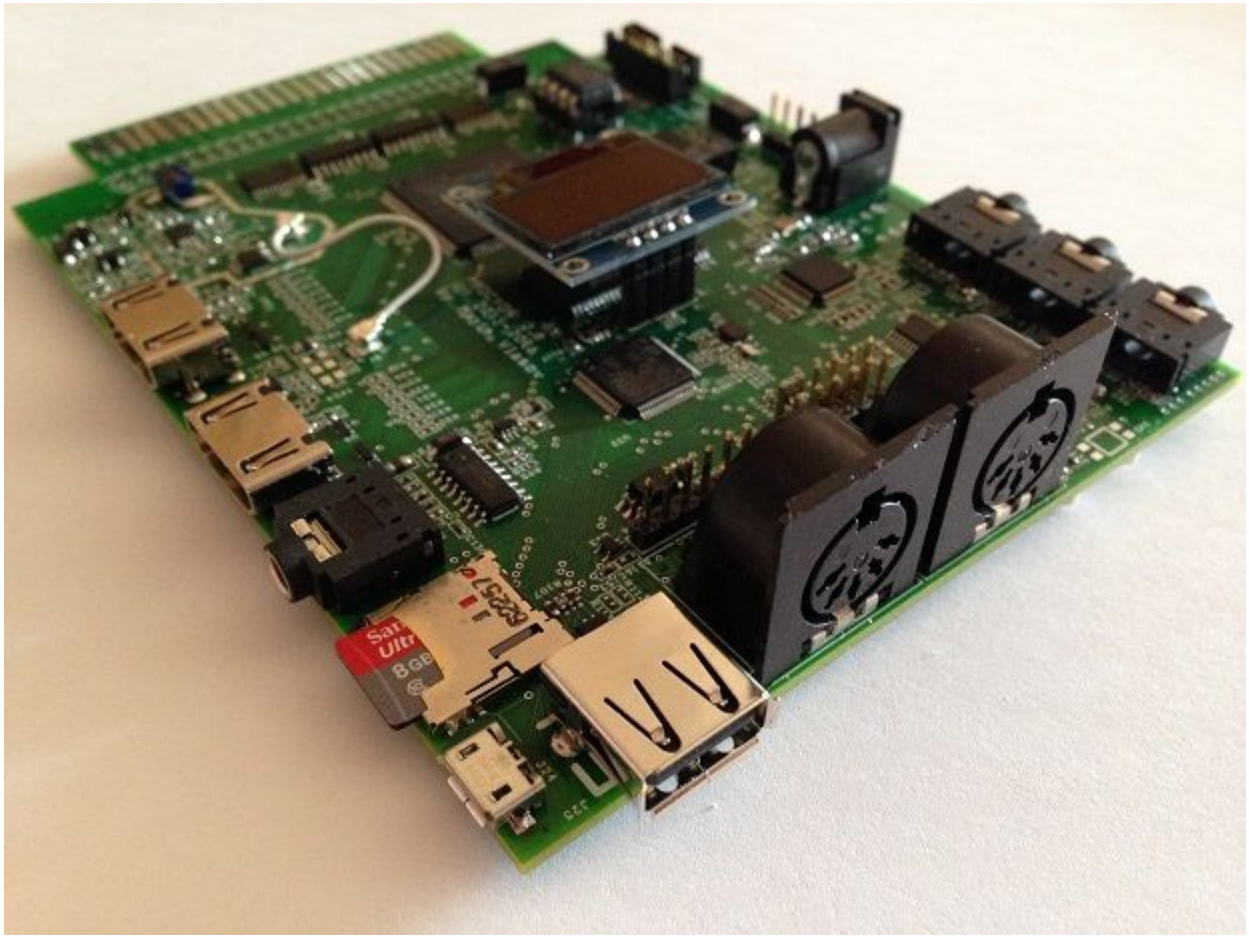
Such a setup is depicted on the diagram below:



The detailed low level operation in the stand-alone mode and is described in the HW chapters.

Procyon Board Architecture

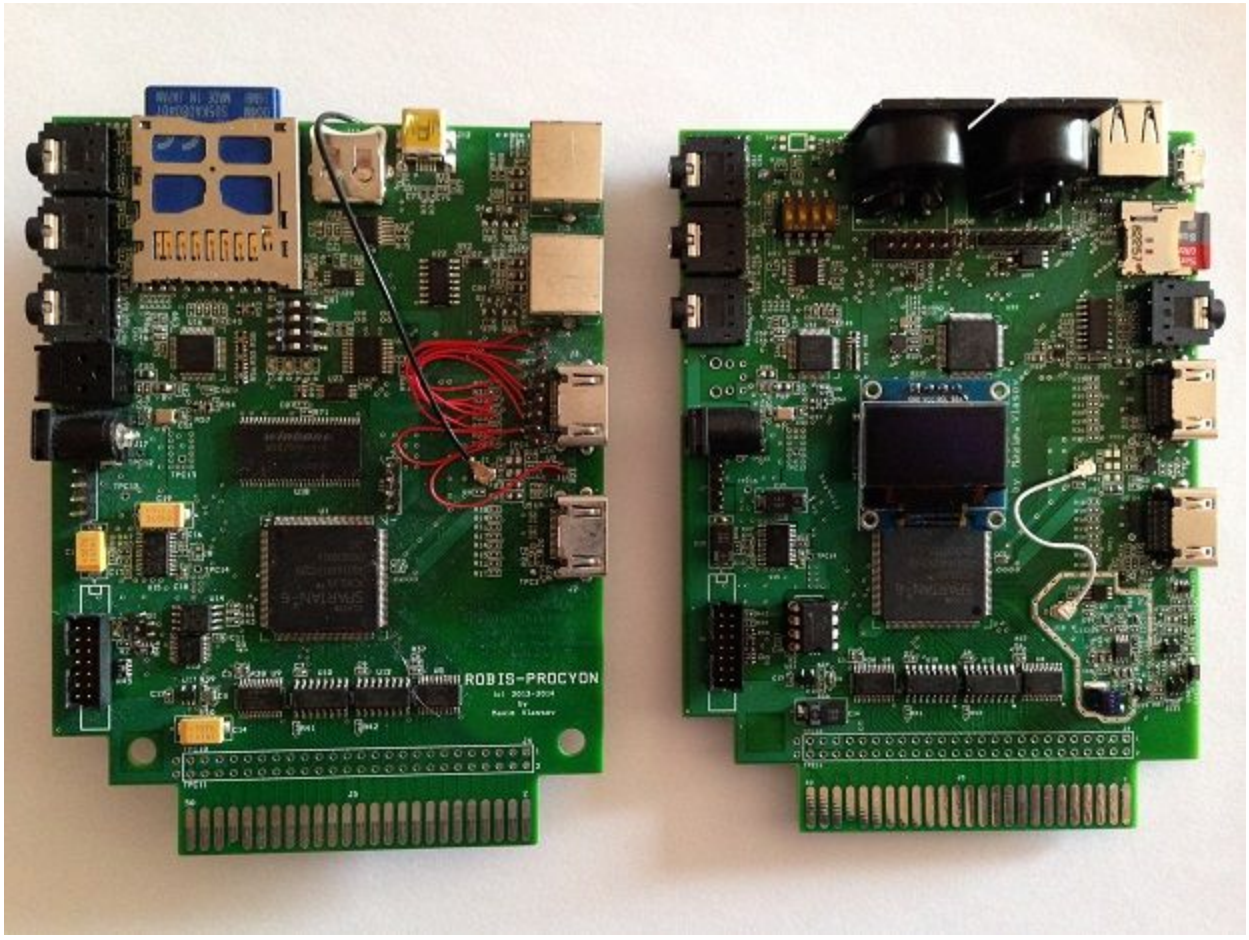
The board is based on the low cost and yet powerful Xilinx Spartan 6 FPGA family. The system is assembled on an inexpensive 13x10cm two layer PCB.



The basic Procyon board features are listed below:

- Xilinx Spartan 6 FPGA XC6SLX9 with 64KBytes of embedded block RAM, 16 DSP slices and more than 11K Flip-Flops available;
- 64 MBytes of SDRAM @ 133 MHz;
- 16 MBytes of the FLASH ROM (FPGA configuration, MSX ROMs and user data);
- 2xHDMI ports – either 2x OUT or IN+OUT configuration;
- AC97 stereo codec with analog Line In/Out+Heaphones;
- TOSLINK (optical SPDIF) output;
- ARM Cortex M4 house keeping controller;
- RTC emulation & replaceable LI battery;
- SD CARD interface;
- USB upstream port for the host connectivity;

- USB downstream port for the HID control devices (mice and keyboards);
- Two switching MIDI ports;
- 100 MHz clock distribution system;
- External 5V power adapter connector;
- Parallel high speed mezzanine connectors 29 I/O + 9 inputs with level shifters;
- Fast I2C bus for the extensions purposes;
- MSX slot connector;
- Precise genlocked PLL.



Spartan 6 Xilinx FPGA is a very popular, versatile, inexpensive and yet powerful family of the programmable logic devices. It was selected for its lowest specific cost per logic gate and excellent performance index. This FPGA sports the special dedicated very high speed peripheral interface, which is used by the HDMI standard. This physical interface is called TMDS (Transition Minimized Differential Signalling).

Due to the presence of TMDS, it became possible to reduce the number of on-board components and completely eliminate the external HDMI physical interface ICs.

The maximum device size in the non-BGA package is limited to 11K Flip-Flops, which is sufficient for the minimum MSX1 system implementation including the CPU or all the MSX compatible peripherals excluding the CPU.
In order to keep the PCB cost and assembly complexity low, the BGA (Ball Grid Array) packaging was discarded in the design process. This is how, such a complex design can be implemented on the 2 layer PCB.
However this advantage brings quite a tough constraint applied to the system architecture. The design is I/O limited and FPGA resource limited.
The following work-around was found in order to implement all the functionality and still keep and low I/O count package:

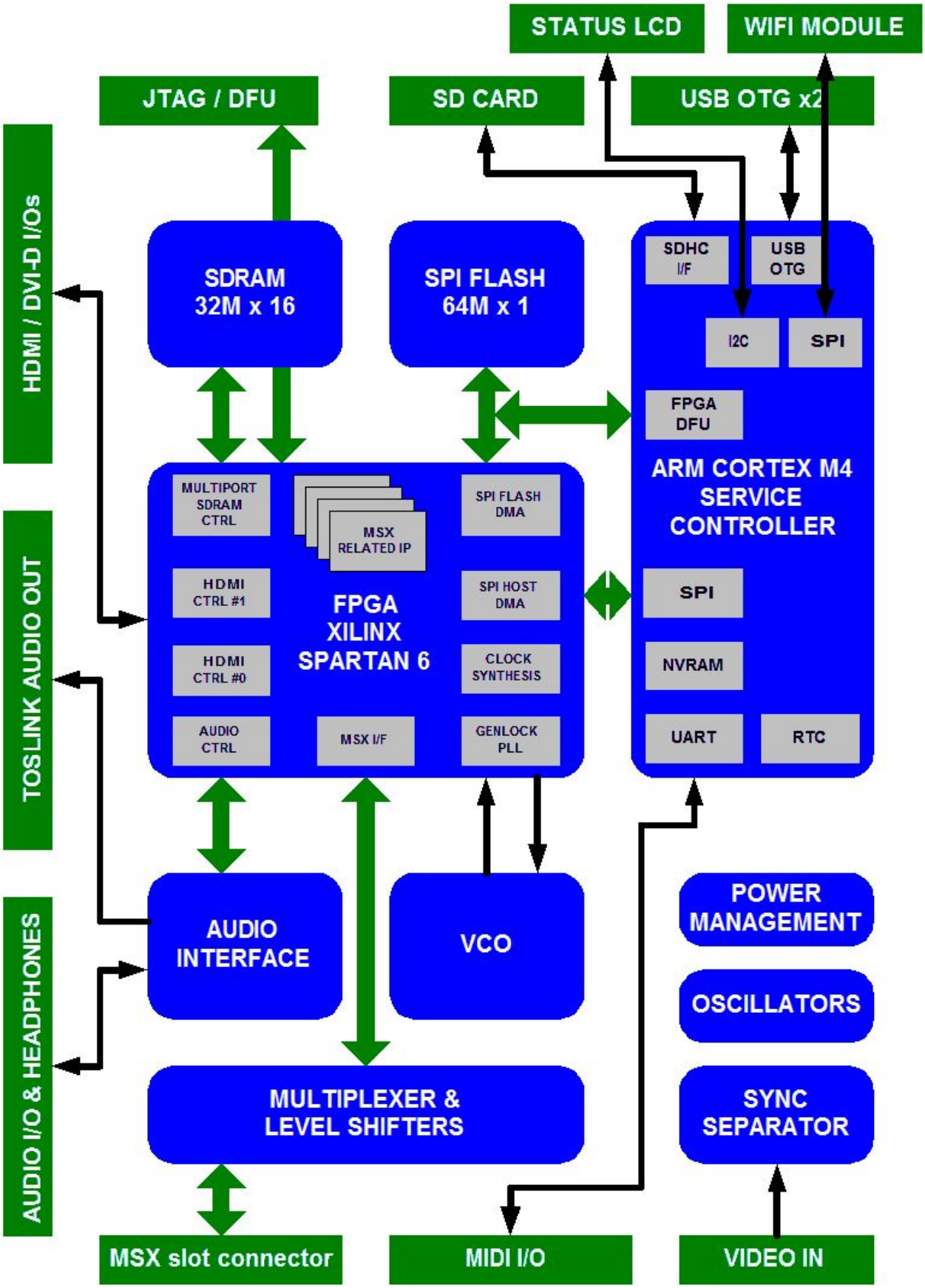
- MSX slot is multiplexed in order to reduce the I/O usage;
- SRAM memory is dropped and instead the 16 bit high performance SDRAM interface is implemented with the multiplexed address bus;
- Digital audio front-end is using AC97 type CODEC with the minimum pin count;
- FPGA configuration code and user ROM are placed into the same device;
- Using the host controller for house keeping functions;
- MIDI, SDHC, WIFI and USB are handled by the dedicated house keeping controller

Hence by extensive usage of the bus multiplexing technique allowed to connect all the required peripherals despite very limited amount of free I/O pins.

The system integrates the ARM Cortex M4 service controller for the house keeping.
The service controller handles the most of the non real time complex functions, including the USB OTG port support, SDHC, RTC emulation and program settings. The uC is connected via the SPI bus to the FPGA.
USB OTG (On The Go) port can act as the upstream and downstream interface. When working as downstream, the HID (Human Interface Device) stack is loaded and the uC runs as the keyboard/mouse USB host.
This is very useful for the computers having no or broken original keyboard/mouse. The BIOS patch is installed and the standard keyboard and mouse handler are replaced. The external keyboard and mouse are supported wherever the software does access the it via MSX BIOS. Some software, mainly game titles incorporate the keyboard scanning routines, not using the MSX BIOS. In such a case, the keyboard/mouse support is not provided.

Also the SDHC pre-formatted in FAT32 is supported by the uC. The physical interface is handled by the uC built-in HW SDHC core and the DSK disk image files are supported directly. SDHC byte stream can be also sent via the audio or video DMA directly to the emulated VDP memory buffer and/or the audio stereo channel.

The Procyon board simplified architecture is depicted on the block diagram below:


STATUS LCD
WIFI MODULE
JTAG / DFU
SD CARD
USB OTG x2
HDMI / DVI-D I/Os
SDRAM
32M x 16
SPI FLASH
64M x 1
SDHC
I/F
USB
OTG
I2C
SPI
FPGA
DFU
ARM CORTEX M4
SERVICE
CONTROLLER
MULTIPORT
SDRAM
CTRL
MSX
RELATED IP
SPI FLASH
DMA
HDMI
CTRL #1
FPGA
XILINX
SPARTAN 6
SPI HOST
DMA
SPI
TOSLINK AUDIO OUT
HDMI
CTRL #0
CLOCK
SYNTHESIS
NVRAM
AUDIO
CTRL
MSX I/F
GENLOCK
PLL
UART
RTC
AUDIO
INTERFACE
VCO
POWER
MANAGEMENT
OSCILLATORS
AUDIO I/O & HEADPHONES
MULTIPLEXER &
LEVEL SHIFTERS
SYNC
SEPARATOR
MSX slot connector
MIDI I/O
VIDEO IN

Power Management

Procyon board is powered by a single +5V power supply. The power is either delivered via the MSX SLOT connector or via the on-board dedicated power connector. There are 3 linear regulators on the board serving for the following purposes:

- The main high current 3.3V regulator is powering the principal power domain to which all the 3.3V ICs are connected for exception of the discrete VCO (Voltage Controlled Oscillator) parts;
- The low noise 3.3V regulator supplies the discrete VCO with a very low ripple and low noise power.
- The secondary 4.1V regulator provides a specific clamp voltage for the level shifting transistors.

The main 3.3 regulator generates the POWER GOOD signal, which is fed to the FPGA configuration start event.
On the power up, when the output voltages reach the required level, the POWER GOOD is set and FPGA configuration procedure begins.

Clock Distribution

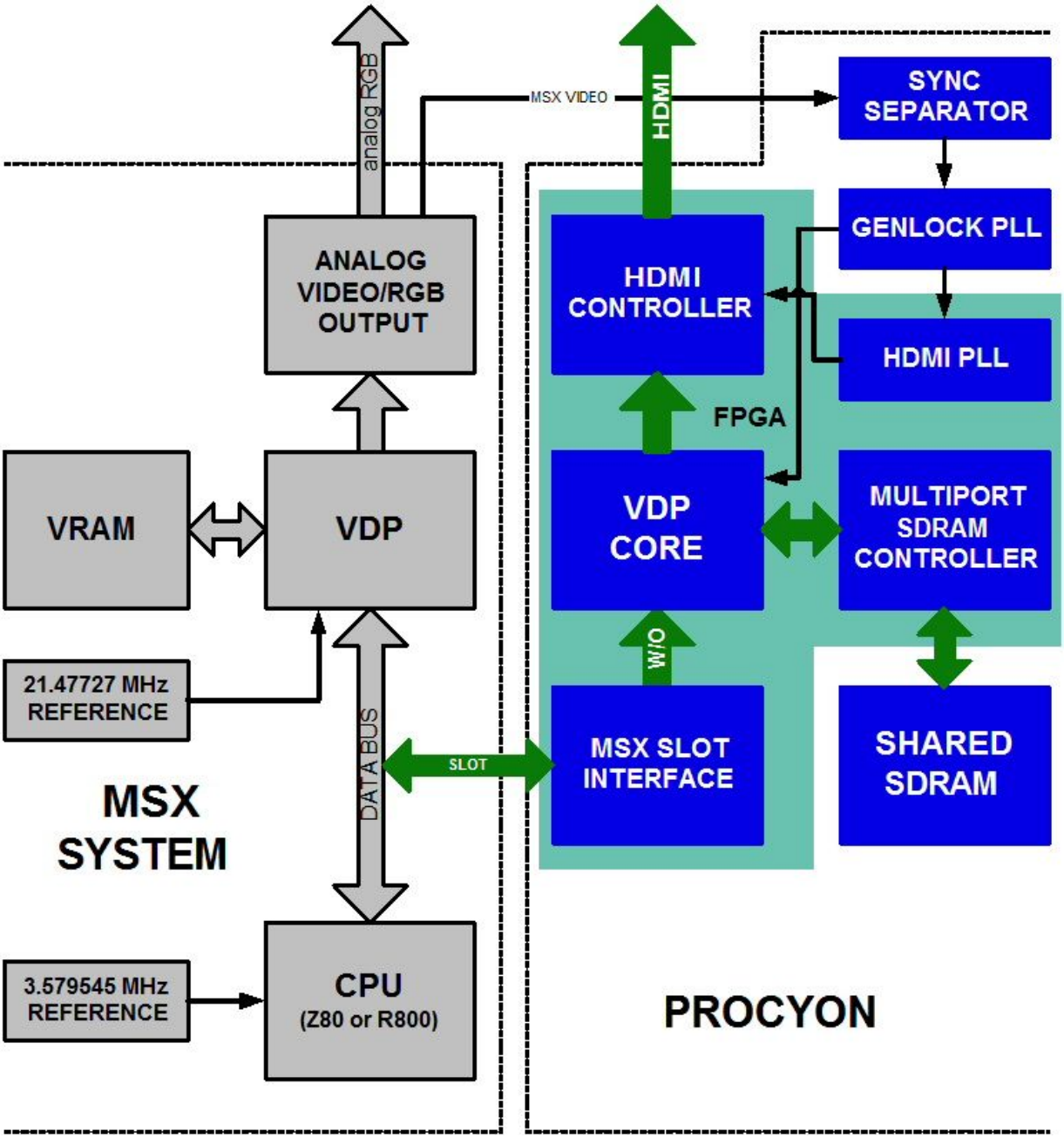
There are several clock sources on the Procyon board. The main oscillator is 100 MHz. This clock source is utilized by the internal FPGA DCMs (Digital Clock Managers, which hold internal PLLs) to generate a grid of fixed frequency clocks.
For example 160 MHz / 133 MHz or 100 MHz clock can be selected to drive the high performance SDRAM controller soft IP core inside FPGA.
Audio CODEC IC incorporates its own crystal oscillator 24.576 MHz. The 3.579545 MHz clock reference is synthesized and applied to the emulated by FPGA audio hardware cores.
There is a 8 MHz built-in crystal oscillator into the STM32F407 ARM Cortex M4 uC. The uC internal clock references, core and peripheral clocks are derived from this time base.
Another clock source is driving the RTC part of ARM uC. 32.768KHz time reference is running contiguously from the battery backup.
The VCO (Voltage Controller Oscillator) ultra low noise and low jitter oscillator generates the clock source utilized by the HDMI output video DMA. This VCO is a part of the PLL locked to the incoming video signal from the MSX host computer. The VCO tuning range is sufficient to detect and lock on all the MSX screen modes with a 5% (50000 ppm) margin.

FPGA Configuration

Xilinx Spartan 6 FPGA uses the SPI FLASH memory for the configuration and user data storage. The FPGA configuration uses approximately 512 KBytes. The rest is available for the user data, ROM storage and programs.

By using the Xilinx Impact SPI FLASH can be programmed either directly or by the JTAG interface and the dedicated SPI programmer IP loaded into the FPGA. This way all the available programming cables are supported.
Once the SPI FLASH holds the valid configuration, it can be updated via the DFU (Device Firmware Upgrade) utility run on the MSX computer. In this case, the new FPGA configuration image must be stored on the SD card.

Video Genlock and PLL

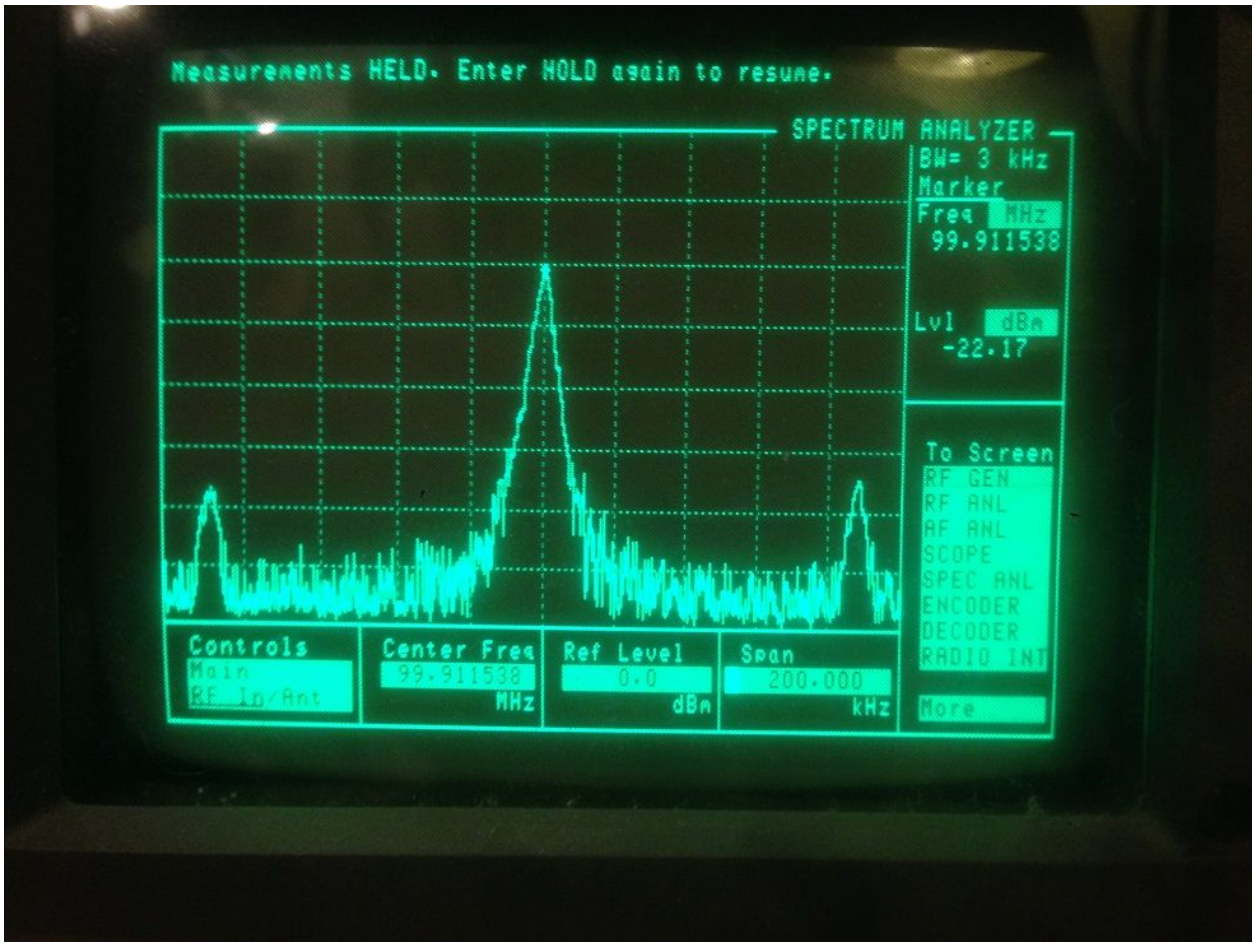


As presented on the diagram above, MSX computer is connected to Procyon board via MSX slot connector and video output connector. All the video data is stored in the native local VRAM (Video RAM) connected to the VDP (Video Display Processor) of the MSX system. However, every write access control and data to the VDP ports is also present on the MSX slot connector. Procyon MSX Slot Interface module snoops the VDP accesses and performs the coherent memory/command VDP execution. VDP core is a cycle accurate replica of the original MSX VDP processor. It is compatible with TI TMS9918, Yamaha/ASCII V9938 and V9958.
Every single write to the main MSX VDP also goes to Procyon VDP core. Same for the memory write operations, every write to the VRAM also goes to the shared SDRAM of the board. However, when CPU reads VDP, only the original VDP is read in order to avoid the data bus contention.
Same mechanism works for the interrupts, where the built-in MSX VDP generates the interrupts and Procyon VDP doesn't.
Procyon VDP core is fully synchronized to the MSX VDP by the means of the video sync PLL. Composite video signal generated by MSX is fed via the synchronization separator module to the FPGA, which verifies the timing, detects the video output standard and then, tunes up the parameters of the genlock PLL on the fly.
The MSX VDP can operate in 8 different modes:

- PAL, progressive 313 lines per field, 1368 clocks per line;
- PAL, progressive 313 lines per field, 1365 clocks per line;
- PAL, interlaced 312.5 lines per field, 1368 clocks per line;
- PAL, interlaced 312.5 lines per field, 1365 clocks per line;
- NTSC, progressive 262 lines per field, 1368 clocks per line;
- NTSC, progressive 262 lines per field, 1365 clocks per line;
- NTSC, interlaced 262.5 lines per field, 1368 clocks per line;
- NTSC, interlaced 262.5 lines per field, 1365 clocks per line

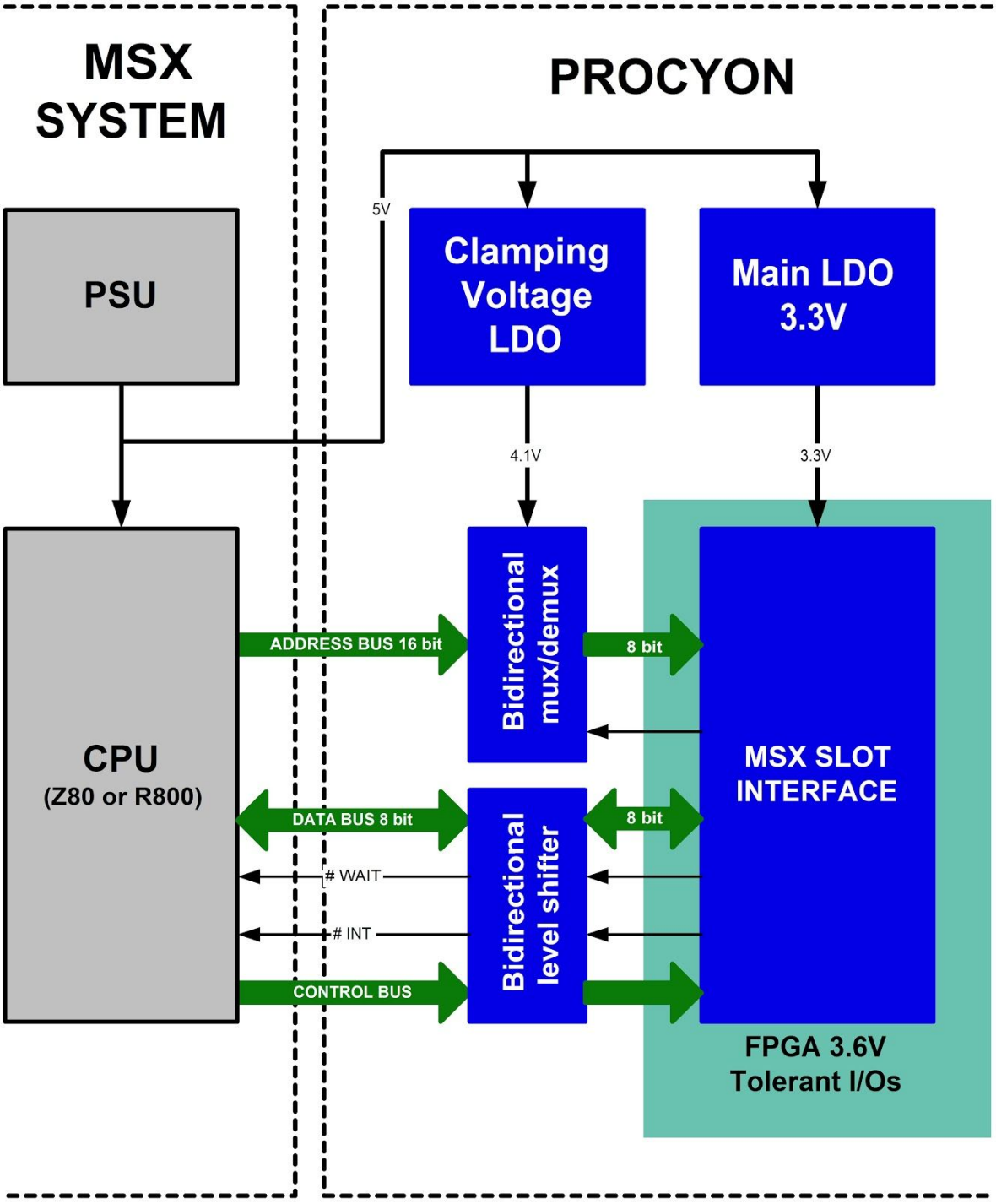
All these modes are fully supported and have a different ratio for the HDMI output.
All NTSC modes are mapped onto the standard VGA mode 640x480 @ 60Hz and all PAL modes are mapped onto the standard SDTV mode 720x576 @ 50Hz.
Also, progressive and interlaced modes have a different number of scan lines per frame. This difference is accounted in the HDMI raster generation.

The HDMI controller core incorporates the 2 horizontal lines memory buffer. Hence the HDMI video is lagging behind the MSX video for one full horizontal scan line (64us).
Interlaced modes are flicker fixed. In other words odd and even fields coming out of MSX VDP are recombined for the full progressive screen with a double vertical resolution.
The analog components of genlock PLL such as low jitter VCO and active loop filter are placed on the Procyon board and powered by the low noise LDO regulator.



MSX Slot Interface and Level Shifters

MSX CPU like the rest of motherboard digital electronics is powered by 5V supply. MSX slot digital signals are also 5V tolerant TTL/CMOS.



The modern digital components, however, do operate at the highest voltage of 3.6V. Procyon uses 3.3V as the main supply. Therefore, the bus level conversion is performed on the board, to ensure the correct signal integrity and ESD protection.

Bidirectional level shifters based on the N-channel silicon gate bypass transistors without an intrinsic diode are chosen. These level shifters require no control and perform bidirectional bus adaptation. The only constraint is the necessity of the clamping voltage, which is 0.7V higher than the maximum I/O LVCMOS level. Hence, 4.1V is selected for the clamping LDO.

SDRAM Interface

SDRAM (Synchronous Dynamic RAM) is chosen as the main storage for various reasons. It was important to find a memory with a low pin count and fast context switching.
All the emulated MSX memory resources, including VDP VRAM, main 4096K of memory mapped RAM and ROM are all mapped to the SDRAM address space. These memory resources occupy independent, separate memory zones, which are grouped in banks.
The bank memory partitioning is extensively used by the SDRAM core controller achieving the short access time latency for each of partitions and having a burst speed beyond 200 MBytes/s.
16 bit data port is optimal for the data granularity, bandwidth and the pin count.
32 bit interface is considered non-economical.
ROM emulation is performed by the one-shot serial DMA controller, which loads some zones of the SDRAM from the configuration SPI FLASH based on the stored user-defined partition table at the system power up event.
Later, these memory zones are accessible via MSX slot interface as the read only memory or ROM.

NVRAM, RTC and USB

Non-volatile RAM, RTC and USB functions are handled by the service uC, based on the STM32F407 ARM Cortex M4 core.
Also, this microcontroller provides the fail-safe FPGA DFU mechanism. I.e. whenever the DFU fails and power is cycled, FPGA not-ready status is generated and uC re-programs the ROM by loading the default FPGA configuration file.

HDMI Interface

HDMI/DVI-D interface is entirely based on the Xilinx Spartan 6 FPGA high speed TMDS physical interface. The external circuitry includes the ESD protection and the optional EDID access (the latter is handled by the house keeping uC). Hot plugging is possible.
The I2C interface is supported by the soft IP module inside the FPGA.
Resolution up to 1080p is ensured by the signal integrity.
Special care was taken at the PCB design phase. The electrical length of the HDMI signals, the capacitive parasitic load and transmission line impedances are carefully balanced.
Due to the aforementioned techniques, the 2 layer PCB construction is sufficient for the HDMI PHY implementation.

Audio CODEC

Audio CODEC (Coder Decoder) is a versatile audio 20 bit ADC/DAC and mixer interface running at the fixed 48 KSamples/s sampling rate. The clock reference of 24.576 MHz is used throughout the audio design. The downsampling converter, audio DMA, antialiasing output filter and the serializer/deserializer are run from this time base.
The Audio CODEC also incorporates the headphone amplifiers to drive the standard stereo headphones.
The standard optical digital audio interface can be used to transport the HI-FI audio content in the non-compromised quality via the fiber optical link to the external audio DAC or home cinema amplifier.
Also there is a line stereo input, which is digitized and intermixed with the internal digital audio sources.
This line stereo input can be connected to the audio synthesizing hardware, not emulated by the Procyon card (like Yamaha SFG-01, Yamaha SFG-05, moonsound etc).

MIDI Interface

MIDI (Music Instrument Digital Interface) is emulated by the FPGA soft core controller replicating MSX Audio (Philips NMS1205) or Panasonic FS-A1GT MIDI hardware.
There are 2 standard ports - IN/OUT..

Rev 1.0 of Procyon board doesn't integrate the MIDI physical interface including the optocoupler and the open collector transmitter. Instead the active cable is used. Currently only the level shifting and ESD protection is placed on Procyon board.

Starting from Rev 2.0, the standard MIDI physical interface is located on the board providing the galvanic isolation from the MIDI equipment.

LCD OLED Status Display

The current board operating status is displayed on the 128x64 pixels OLED display situated in from of the board. The status reflects the FPGA and peripheral operating modes and it's updated in real-time in accordance to the user actions. If the FPGA DFU fails, the status is displayed and the user is asked about FPGA image DFU backup action.

FPGA Design/Soft IP Cores

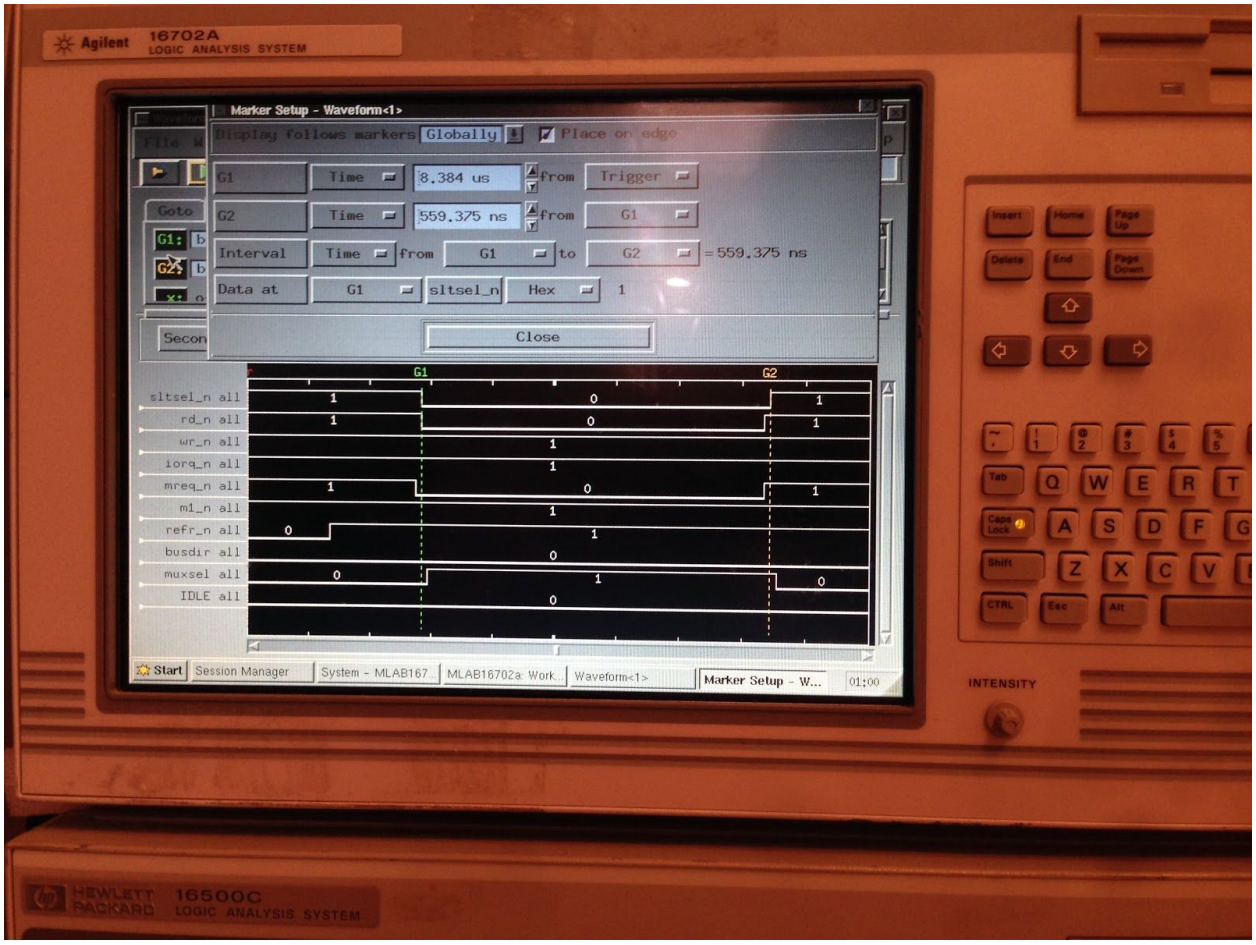
The entire FPGA project was implemented in Verilog (IEEE 1364) HDL (Hardware Description Language). The top level design wrapper integrates the FPGA device specific instances and hardware IP modules. However, all the soft IP cores are technology independent and can be integrated into any modern FPGA or ASIC.

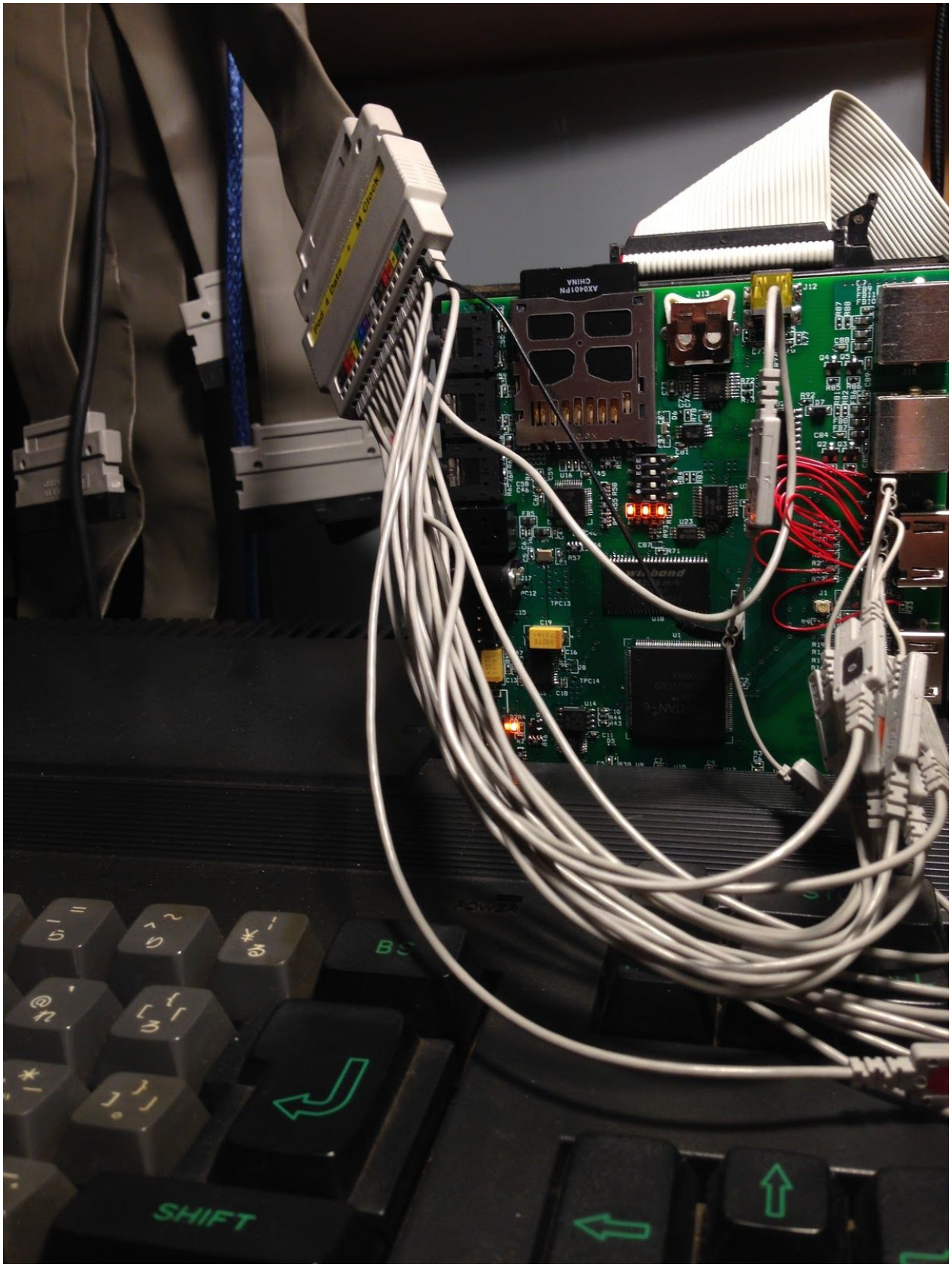
HW Signal Integrity and Compliance Testing

Extensive signal integrity testing was performed on the slot interface. The compatibility of the logic levels was ensured by the active level shifter design.
The timing specification outlined in the MSX Technical Data Book, MSX2 Technical Handbook was integrated into the FPGA testbench verification environment.
Then, after the FPGA synthesis and the gate-level simulation, the timing integrity was verified by the regression testing using the versatile Logic Analyzer setup (Agilent 16702a) .
Timing errors were found and fixed until the full compliance was achieved.
The board inter-operability was verified also in many MSX computers, including:

- Yamaha YIS503II, CX5MII, CX5MII/128, CX11, YIS503/III, YIS805;
- Toshiba FS-TM1;

- Panasonic FS-A1ST

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